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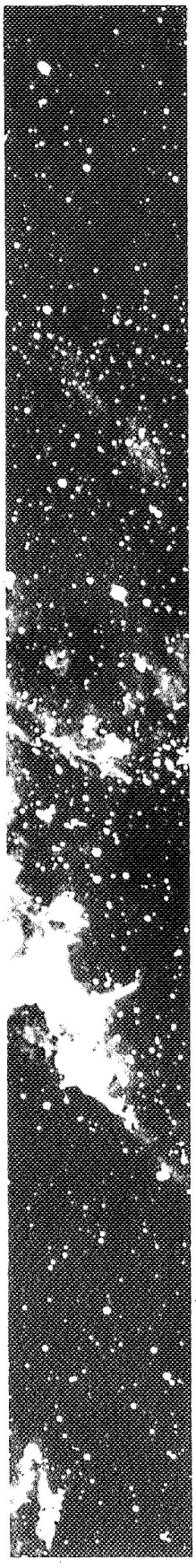
15 DECEMBER 1969
NASA-CR-108784

SPACE SYSTEMS



POWER CONDITIONING EQUIPMENT FOR A THERMOELECTRIC OUTER PLANET SPACECRAFT POWER SUBSYSTEM

QUARTERLY TECHNICAL REPORT

JPL CONTRACT NO. 952536

GENERAL ELECTRIC

1J86-TOPS-480
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POWER CONDITIONING EQUIPMENT

FOR A

THERMOELECTRIC OUTER PLANET SPACECRAFT

QUARTERLY TECHNICAL REPORT

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GENERAL ELECTRIC COMPANY
VALLEY FORGE SPACE CENTER
P. O. BOX 8555
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"THIS WORK WAS PERFORMED FOR THE JET PROPULSION LABORATORY, CALIFORNIA INSTITUTE OF TECHNOLOGY, AS SPONSORED BY THE NATIONAL AERONAUTICS AND SPACE ADMINISTRATION UNDER CONTRACT NAS 7-100."

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ABSTRACT

This report covers the analysis of requirements and the detailed circuit design phase of the power conditioning electronics for a nuclear powered outer planet scientific spacecraft with a twelve year life. A study was completed to identify an optimum frequency range for operation of electronic power processors, and a comparison was made of three candidate electrical power distribution configurations. The electrical design of a two phase inverter, a quad redundant shunt regulator, a DC to DC converter, and typical power switching circuits was advanced and detailed schematics are presented. Additionally, the electronic piece parts of the front end of a Jensen oscillator were packaged utilizing thick film microcircuit techniques for improvement.

The objective was a design to provide regulated power for engineering and science subsystems from a radioisotope thermoelectric generator, and to perform switching and control functions for the effective management and distribution of electrical power. The baseline electrical power subsystem established provides an optimized design to match the power source with the electrical loads, and also provides Peltier cooling at all times to extend thermocouple life.

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INTRODUCTION AND SUMMARY

This Quarterly Technical Report for the period 1 July 1969 through 30 September 1969 was prepared in accordance with Article 2.(c)(3) of Jet Propulsion Laboratory Contract 952536.

SUBJECT OF REPORT

The report covers activities of the second quarter, consisting primarily of detailed design of the electronic circuits to meet subsystem requirements; and a parallel effort to analyze the system and subsystem requirements to define an optimum frequency for power conditioning and the most desirable form of electrical power distribution.

OBJECTIVES

The objective of this work is to develop, design, and test new technology, circuits, processes, and concepts to advance the state of the art in electronic power conditioning equipment and to assure operating times in excess of twelve years. A parallel objective is to design, develop, fabricate and deliver hardware for integration and test.

WHY WORK IS BEING DONE

This work is being done to optimize power conditioning equipment and to assure compatibility between the radioisotope thermoelectric generator and the spacecraft loads, and to develop confidence in meeting the twelve year life requirement of interplanetary missions.

CONCLUSIONS

Interim conclusions are that the design must be versatile to meet the conflicting requirements of optimized design, vehicle constraints, and continuing change.

RECOMMENDATIONS

The designs applicable to the twelve year life requirement based on previous space power experience require significant sophistication and improvement to demonstrate confidence in successful mission completion.

SIGNIFICANCE

This effort is significant for long duration planetary missions since the equipment must be made free of failures, be capable of continuous satisfactory performance after experiencing a failure or have autonomous emergency adaptability characteristics. This capability is not presently within the state of the art of power conditioning design, but must be developed and demonstrated.

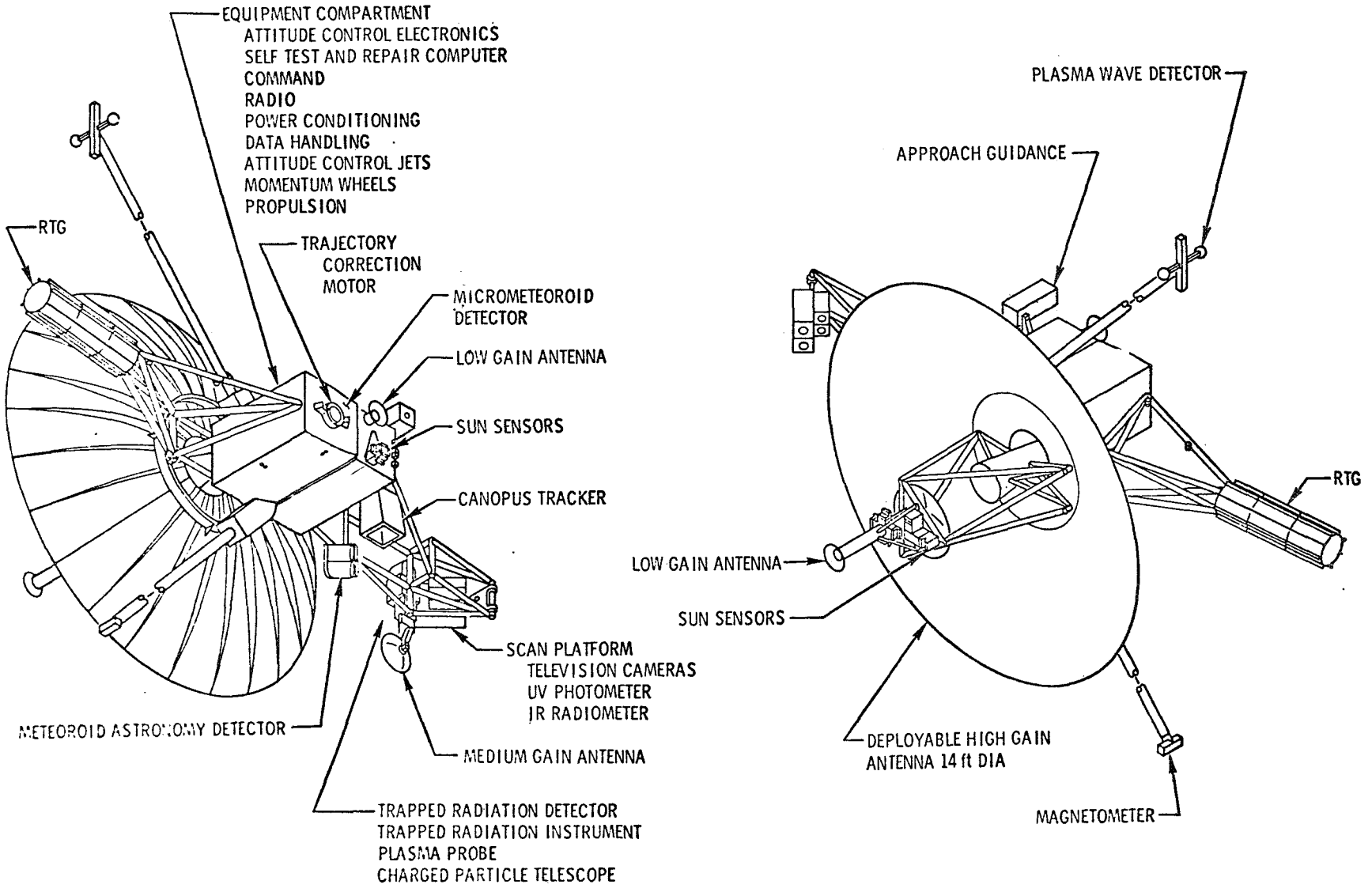
TECHNICAL DISCUSSION

SECTION 1. SYSTEM SUMMARY

The Thermoelectric Outer Planet Spacecraft (TOPS) mission is a minimum launch energy, gravity assisted tour of the outer planets; Jupiter, Saturn, Uranus, and Neptune; during the unique planetary alignment period that exists in the 1976-1980 time period.

The launch vehicle configuration, operational modes, baseline grand tour trajectory, and representative encounter events were defined in the First Quarterly Technical Report, 1J86-TOPS-479 dated 15 October 1969. The latest equipment arrangement is shown in Figure 1-1, Baseline Spacecraft (S/C) Configuration.

THERMOELECTRIC OUTER PLANET SPACECRAFT
CONFIGURATION 12J



1-1. Baseline Spacecraft Configuration

TECHNICAL DISCUSSION

SECTION 2. DESIGN REQUIREMENTS AND CONSTRAINTS

The Power Conditioning Equipment (PCE) design requirements and constraints were defined and listed in the First Quarterly Technical Report, 1J86-TOPS-479 dated 15 October 1969. Since that time, the study contract for the Radioisotope Thermoelectric Generator (RTG) was awarded, and the specific performance was raised from the previous 1.2 watts per pound at outer encounter to 1.7 watts per pound.

The combined power capability of the generators at beginning of Mission (BOM) will be in excess of 575 watts, an increase from the previous 500 watts. Power output of the generators will be approximately 440 watts at the conclusion of twelve (12) years of operation, end of mission(EOM), an increase from the previous 416 watts.

TECHNICAL DISCUSSION

SECTION 3. BASELINE POWER SUBSYSTEM

Summary

The Electrical Power Subsystem presented in this section and the circuit configurations presented in Section 4 are based on an analysis of the requirements, and detailed results of studies that are presented in Section 7. The result is the Baseline Power Subsystem shown in Figure 3-1. The blocking diodes at the RTG's have been removed, the Main Inverter has been deleted as discussed in Section 7-2, and the ac power requirements of the Attitude Control System are supplied by a Two Phase Inverter.

Weight Analysis

A detailed weight analysis was performed based on the electronic piece parts of the circuits shown in Section 4. The results are summarized in Table 3-1, indicating that the present equipment is under size but overweight. It should be noted that the Power Distribution Assembly weight is based on a total of 44 switched functions as shown on the Power Flow Diagram, Figure 4-4, and the circuitry to perform each switching function has an electronic piece part weight of 0.195 pounds.

Ground Control of Unswitched Loads

As presently defined, the power conditioning equipment does not have the command capability to remove certain critical subsystems from the main power bus. To date, these subsystems are radio frequency; command; central computer and sequencer; and attitude control electronics and gyro electronics.

During ground testing of the TOPS spacecraft, a situation might arise which would require removal of one of these subsystems from the bus while maintaining ground power (via power conditioning equipment) on the remaining subsystems. This condition could be brought about either by test phasing (i.e., while testing the temperature control subsystem there is no need for the attitude control electronics to be on), or by test failure (i.e., central computer power shorts out while in the thermal vacuum chamber but thermal control must be maintained).

Since these situations are possibilities, it is recommended that ON/OFF switching capability be added to the power conditioning equipment that can only be used for ground test and checkout. A means for implementation is shown on Figure 3-2 . Regulated power is wired from down stream of the shunt regulator, out and back into the PCE through a "Flight Plug" (encapsulated electrical connector with wiring and resistors in it), through an ON/OFF switch (shown for diagram purpose as a relay), and out of the PCE to the normally unswitched load. Control/command

of the switch is wired through the TOPS spacecraft umbilical connector such that once this connector is demated on the pad, the OFF switch cannot be commanded. The switch could also include current sensing to automatically trip open in case of an overload.

To prevent this switch from causing flight problems, the "Flight Plug" used for test is removed on the launch pad, and replaced by one for flight use. This one provides an electrical path which shunts the switch. (See dotted line on the schematic.)

When the switch removes the spacecraft equipment from the main power bus, an equivalent dummy load (located in the flight plug) must be switched in to prevent excessive power dissipation in the shunt regulator.

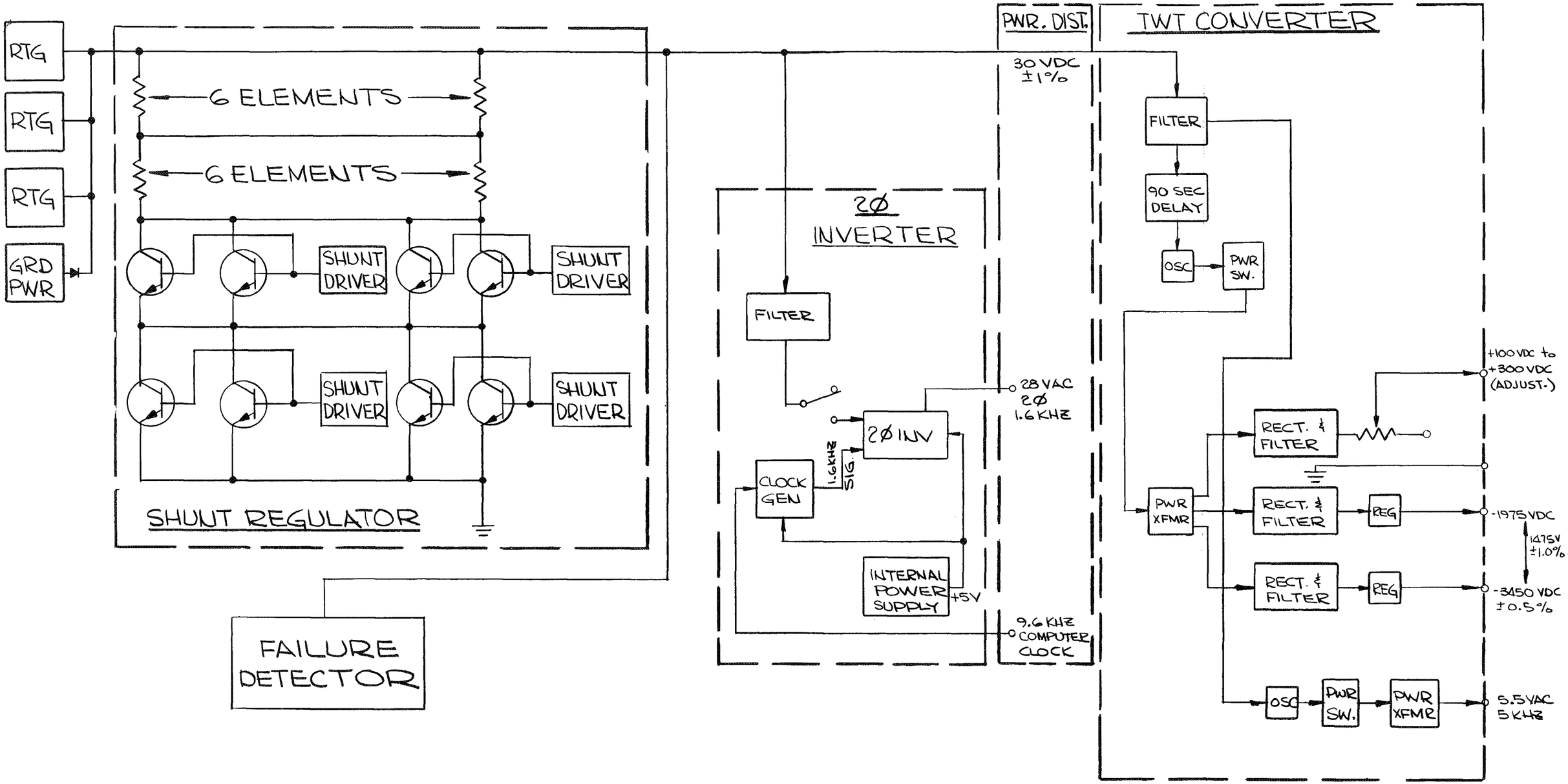


Figure 3-1. Baseline Power Subsystem Block Diagram

Table 3-1. Preliminary Weight Analysis

	Electronic Piece Part Weight	Mechanical Piece Part Weight*	Total Parts Weight	Size	Volume
Shunt Regulator Assembly	2.23	2.50	4.73	2x13x10	260
* Power Source and Logic Assembly	2.00	1.00	3.00	2x4x6	120
Two Phase Inverter Assembly	0.62	1.00	1.62	3x5x13	130
Power Distribution Assembly	8.58	2.50	11.08	4x15x7	420
Chassis, Connectors, Wiring			5.43		255
Total Power Conditioning Equipment Weight, Pounds	13.43	7.00	25.86		1185
Specification Weight, Pounds			14.40	14.5x16x7	1620
TWT Converter Assembly	3.53	3.00	6.53	4x5x10	200

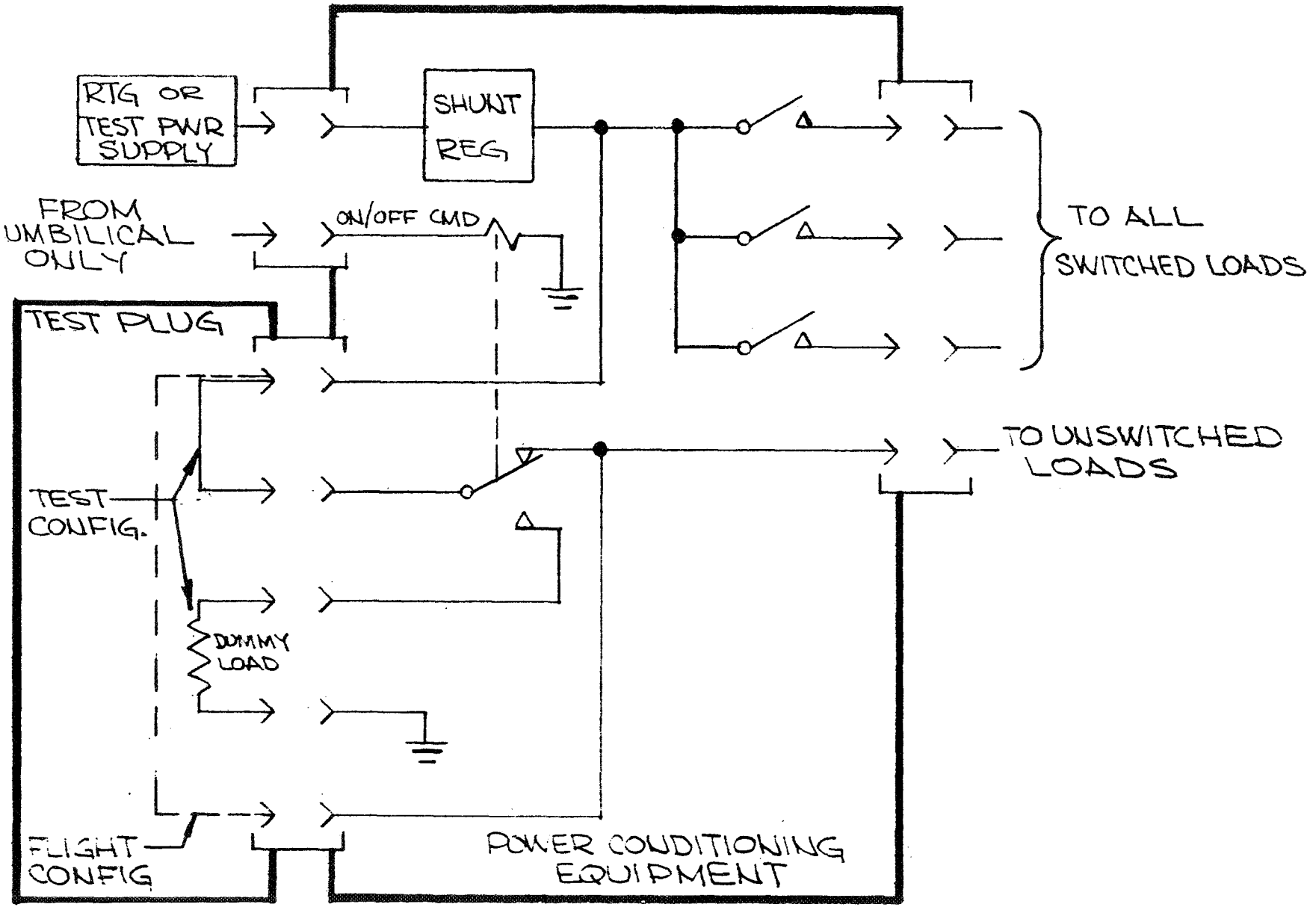


Figure 3-2. Ground Control of Unswitched Loads

TECHNICAL DISCUSSION

SECTION 4. COMPONENT DESCRIPTION

Shunt Regulator Assembly

The shunt regulator maintains a constant voltage bus powered from a radioisotope thermoelectric generator by drawing that amount of extra current from the source to cause the excess voltage to be dropped across the internal resistance of the # thermocouples. For a fixed characteristic source, the shunt regulator furnishes the requirements of the thermoelectric junction to operate at significant current levels, even though the spacecraft loads have a 242 to 428 watt variation. The RTG requirements as a function of mission mode are shown in Figure 4.1.

A reliability analysis presented in Section 7-4 compared the multiple shunt configuration with a quad redundant configuration, and resulted in elimination of the multiple shunt configuration from further study. The present design is covered in the schematic of Figure 4-2, where any one or more of the four elements can control the operation and regulate the bus voltage. The circuit has been breadboarded, and preliminary results show that voltage regulation can be maintained against a load change of 180 watts and a temperature range from 40°F to 100°F, with a total deviation of plus or minus 0.3 percent. Full test data will be provided during the next reporting period.

Power Source and Logic Assembly

This assembly selects the power source from the three RTG's or ground power, provides signal conditioning for telemetry of currents, voltages, and RTG temperature and pressure, and disconnects non-critical loads at system undervoltage.

No effort was expended to further define requirements or implement with circuit designs during the period covered by this report. Preliminary specification is given on Table 4-1, but the only design effort completed is a conceptual design of a voltage protective circuit shown on Figure 4-3. The initial characteristics of the multi-hundred watt RTG indicate that pressure sensing is neither required nor desired, and it is recommended that power conditioning for the pressure transducer be removed from the design requirements.

Power Distribution Assembly

The function of the power distribution assembly is to receive spacecraft commands and to control the flow of electrical power to loads by logically interpreting these commands and operating power switches.

A variety of possible command signal sources were considered during the period covered by this report, and a number of different circuit implementations of power switching were considered. The power flow diagram of Figure 4-4 shows schematically the number and location of these switches as presently defined.

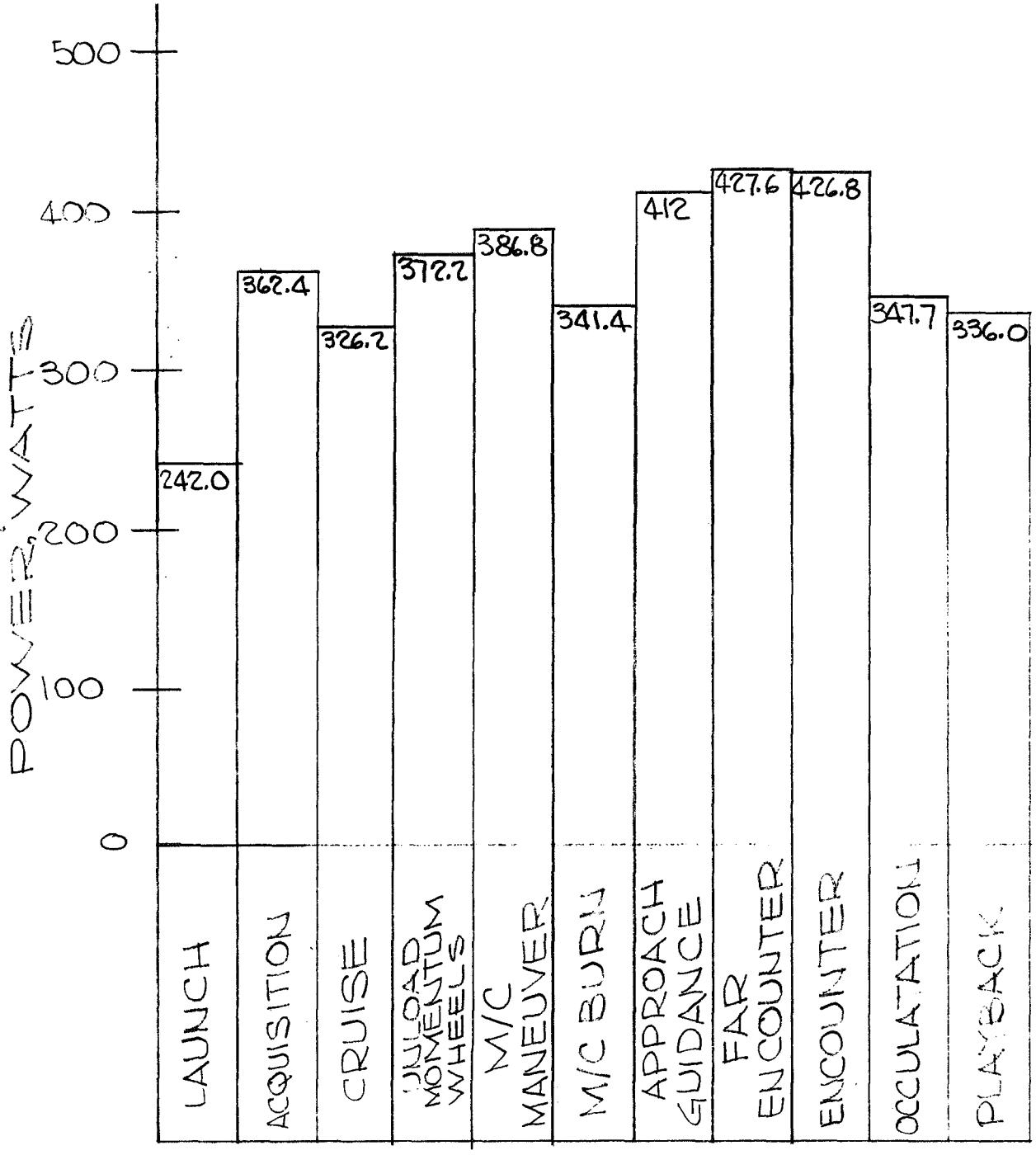
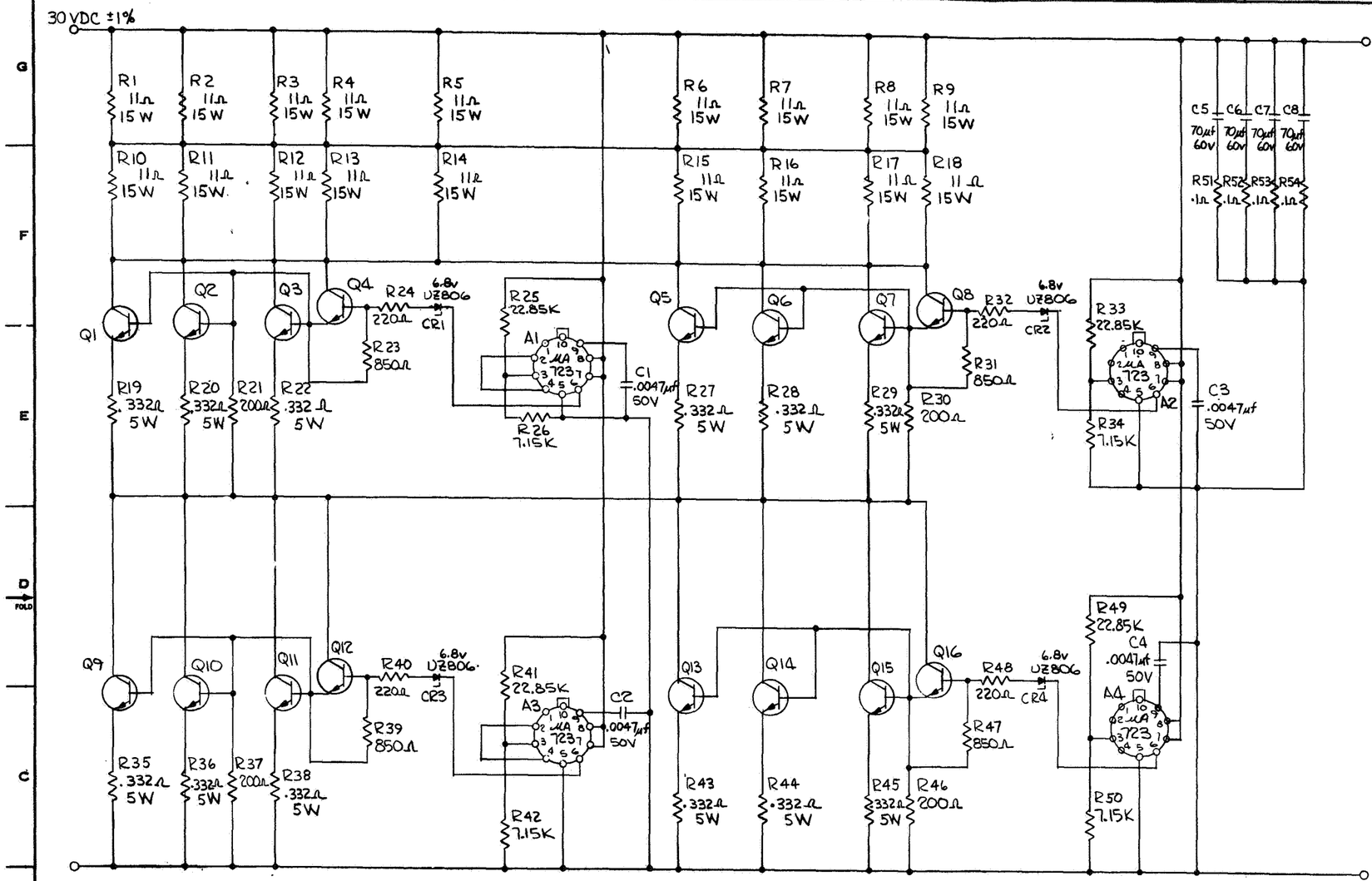


FIGURE 4-1. RTG POWER REQUIREMENTS



NOTES:-

1. UNLESS OTHERWISE SPECIFIED -
   (A.) ALL TRANSISTORS ARE 2N3773.
   (B.) ALL RESISTORS ARE 1/8W.
   (C.) ALL RESISTORS ARE 1%

REVISIONS				
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Figure 4-2. Shunt Regulator Schematic

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES— TOLERANCES ON: 2-PLACE DECIMALS ± 3-PLACE DECIMALS ± ANGLES ± FRACTIONS ± MATERIAL—	ALL SURF. ✓	SIGNATURES	DAY	MO	YR
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		CHECKED			
		ISSUED			
		ENGRG			
		MFG			
		MATLS			

GENERAL ELECTRIC DEPT LOC

TOPS
SHUNT REGULATOR (FLIGHT)

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TABLE 4-1

PRELIMINARY SPECIFICATION, POWER SOURCE AND LOGIC ASSEMBLY

FUNCTIONS

- o Provides control for external power sources
- o Provides current and voltage signal conditioning for telemetry
- o Provides OSE Interface for the Power Subsystem
- o Disconnects non-critical loads at under voltage

PERFORMANCE CHARACTERISTICS

Maximum power dissipation	4.0 watts

PHYSICAL CHARACTERISTICS

Size	2x4x6
Weight	3 pounds

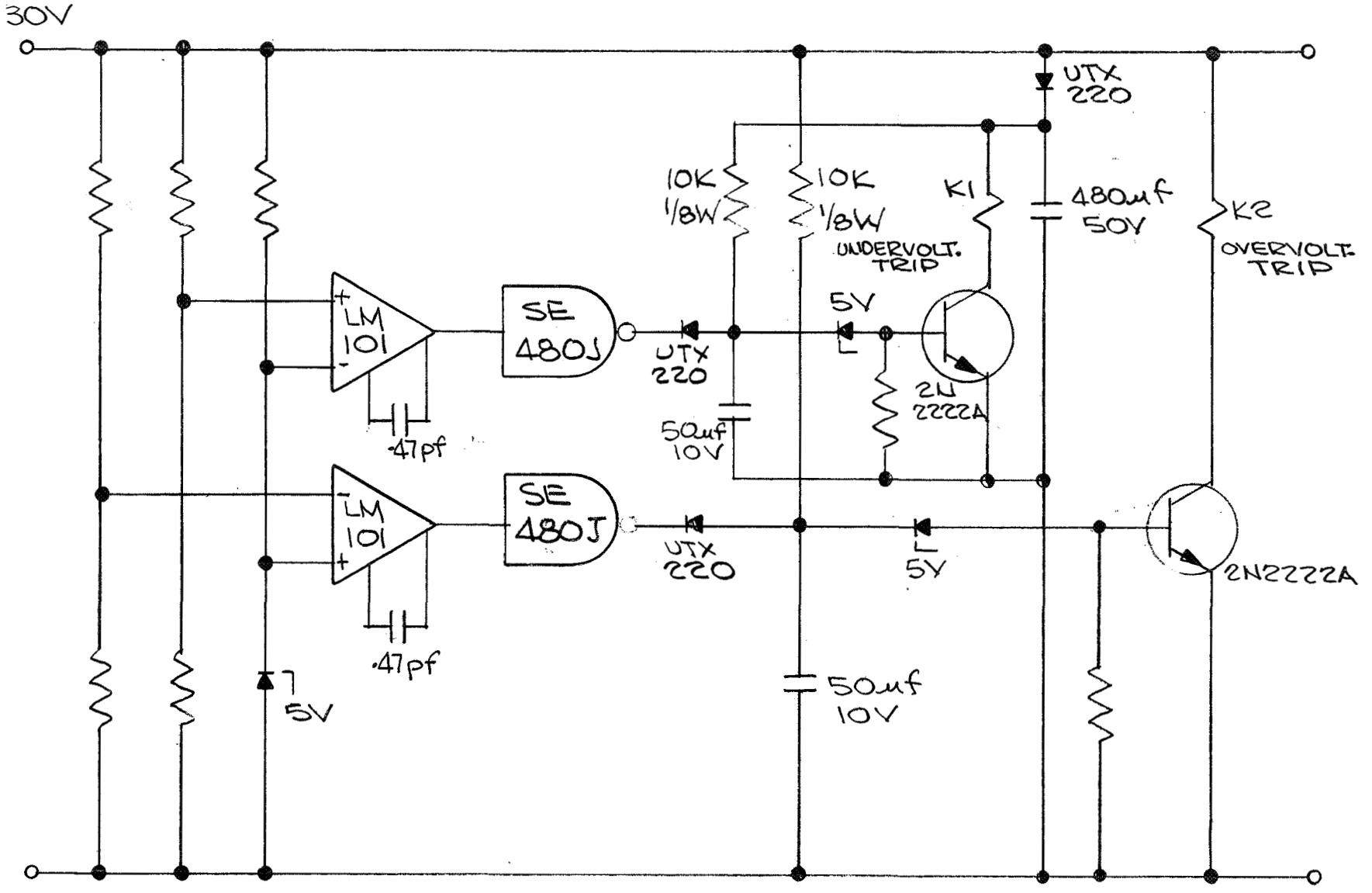

Figure 4-3. Voltage Protective Circuit

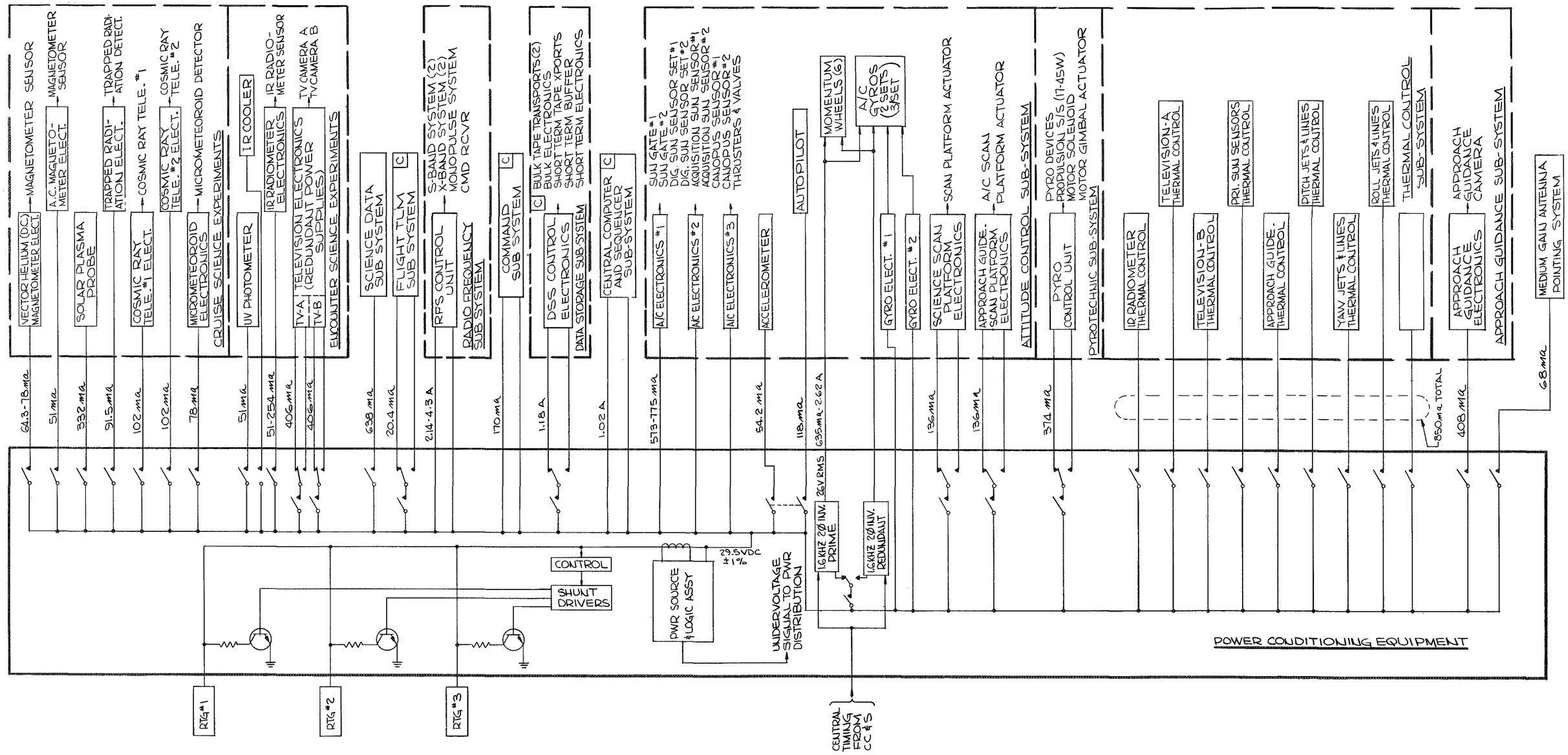

Figure 4-4. Power Flow Diagram

There are two basic considerations which have the greatest influence on the switching design: long life and "no single failure". Both requirements lead to a design incorporating parallel paths. On a spacecraft which has an electrical power limit, it is also necessary to be able to disconnect loads which are not needed to prevent loss of use of loads with a higher priority. Therefore, a "quad" contact arrangement is proposed, shown in Figure 4-5 which provides redundant break capability.

This proposed circuit provides redundancy in the contact, the predominant failure area. Since the proposed switching circuit provides operation even when one relay and/or its driver fails, there is no requirement for redundancy in the drivers. A primary design objective for the drivers is simplicity and low power consumption. The commands are assumed to be pulses with a duration of thirty to one hundred milliseconds at about 24 volts to command, one to two volts no command.

The primary switching relay, K1 in Figure 4- 5, will be switched by a toggle command. The toggle position sense will be off the "back" contact of the primary relay, as shown. The FET sensing circuit for this function uses very little power and has a time constant much longer than the command duration to prevent any possibility of the position sense changing state while the command is still applied. Since the switch will oscillate if the command remains on, the command is AC coupled by capacitors C1 and C2 in Figure 4-5 If the command source is failsafe (the command would never remain on for longer than the specified pulse time) and could provide greater than 1 milliamp at 20-30 volts DC for the command, the capacitive coupling and one stage of amplification could be eliminated to considerably simplify the relay driver. A high voltage signal was assumed so that the circuits can be designed with a high threshold for noise immunity.

In a quad arrangement, if the primary relay is assigned the "sense" on/off, the second relay can only be designated as on or off given the position of the first relay. It is therefore impossible to sense the output for directing a toggle. Accordingly, a different command scheme is proposed for the second relay, shown functionally in Figure 4-5 Each second relay would be individually commanded to achieve state "2" (opposite position shown in Figure 4-5) and a group of second relays would share a single command to put them in state "1". If the primary relay in the quad set failed "open", the load would be turned on by using the command to put the second relay for that load to the "2" state. The load would be turned off by giving the "1" state command to the group which contains the second relay for this particular load. Since the other second relays of the group are in state "1" (the normal state), the only change will be in the second relay which had been set to state "2" to overcome the failed primary relay. If the primary relay failed "on", the load would be turned off by the "2" state of the second relay and on by the "1" state command to the group.

It was assumed the second relays would be commanded from the redundant command source and complete individual load control was required, but an alternative to a toggle command scheme would afford a desirable functional redundancy rather than a block redundancy.

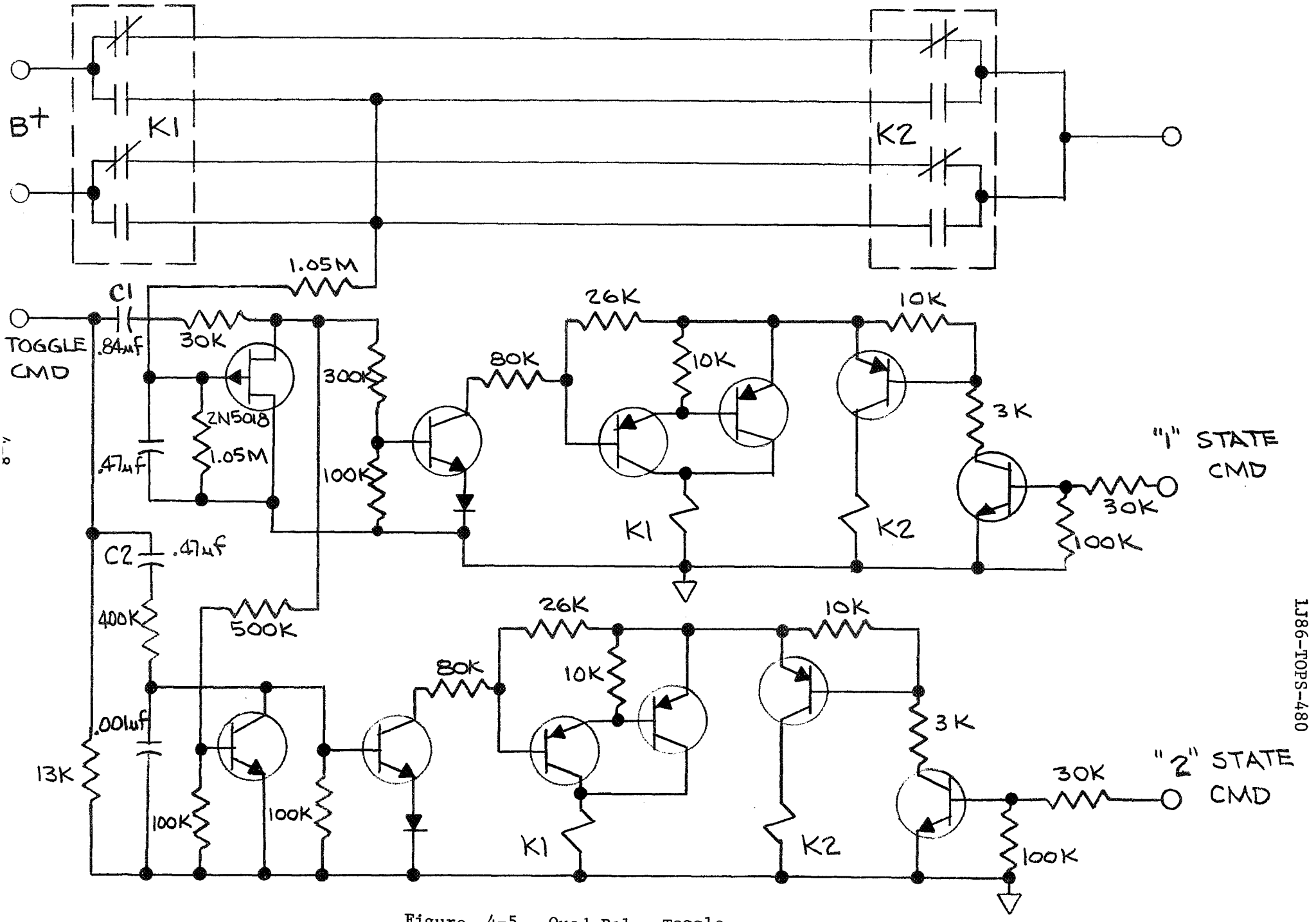

Figure 4-5. Quad Relay Toggle

Two Phase Inverter Assembly

AC power can be provided from a dc to dc converter by a transformer winding directly, without the rectifier and filter stage. However, the dc to dc converter uses an ac link whose frequency is not significant. When ac power is required, it is usually necessary to maintain constant frequency, and more elaborate circuitry is required.

The schematic of Figure 4-6 shows an internal semiconductor clocking arrangement that can be overridden by the central clock of the vehicle to maintain synchronization with other attitude control subsystem functions. The internal oscillator can be adjusted to operate at either 400 Hertz or 1600 Hertz without significant changes. The prominent drawback is that the output voltage follows the input voltage less the saturated transistor voltage drops.

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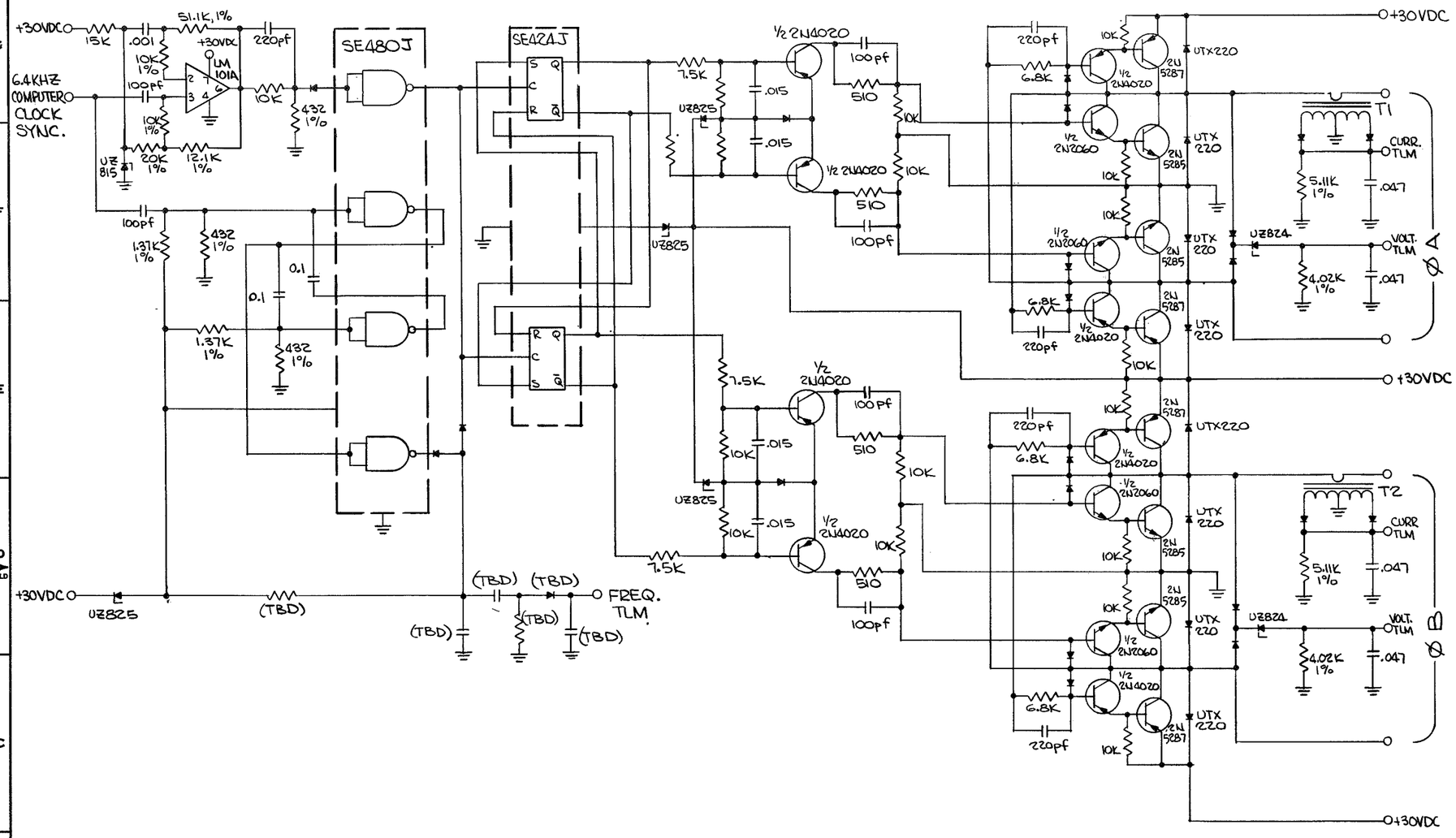


NOTES:-

1. UNLESS OTHERWISE SPECIFIED
   (A) ALL DIODES ARE 1N914.
   (B) ALL CAPACITORS ARE IN MICRO-FARADS.
   (C) ALL RESISTORS ARE IN OHMS, 1/4W, 5%.

Figure 4-6. Two Phase Inverter Schematic

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES— TOLERANCES ON: 2-PLACE DECIMALS ± 3-PLACE DECIMALS ± ANGLES ± FRACTIONS ± MATERIAL—	ALL SURF. ✓	SIGNATURES	DAY	MO	YR
		DRAWN	19	8	65
		CHECKED			
		ISSUED			
		ENGRG			
		MFG			
		MATLS			

GENERAL ELECTRIC — DEPT LOC

TOPS 2Ø INVERTER

SIZE D | CODE IDENT NO. | SCALE ~ | SHEET 1 OF 1 | DIST TO

PN-066-F (1-68) PRINTED IN U.S.A.

SECTION 5. RADIOISOTOPE THERMOELECTRIC GENERATOR

During the period covered by this report, the Atomic Energy Commission let a contract to perform preliminary design studies on a Multi-Hundred Watt Radioisotope Thermoelectric Generator which would have as one of its applications the TOPS mission. The first review of the baseline configuration is tentatively scheduled for mid-November 1969, and results of this contract as it proceeds and needs of TOPS as they become identified will be integrated into both contracts.

SECTION 6. BREADBOARD ACTIVITY

During the period covered by this report, breadboards were fabricated for

Shunt Regulator Assembly
Two Phase Inverter Assembly
TWT Converter Assembly

In addition, electronic breadboards were completed for the following functional circuits:

DC to DC Converter
Power Interface Controller
Static Breaker (Semiconductor)
DC Static Switch (Electromagnetic)
Quad Relay Switch

For the final breakboard set, the following circuits will be mounted as shown on Figure 6-1, and shipped to the Jet Propulsion Laboratory:

A Shunt Regulator
Two 2-Phase Inverters
A Power Source and Logic Assembly
A Power Distribution Assembly

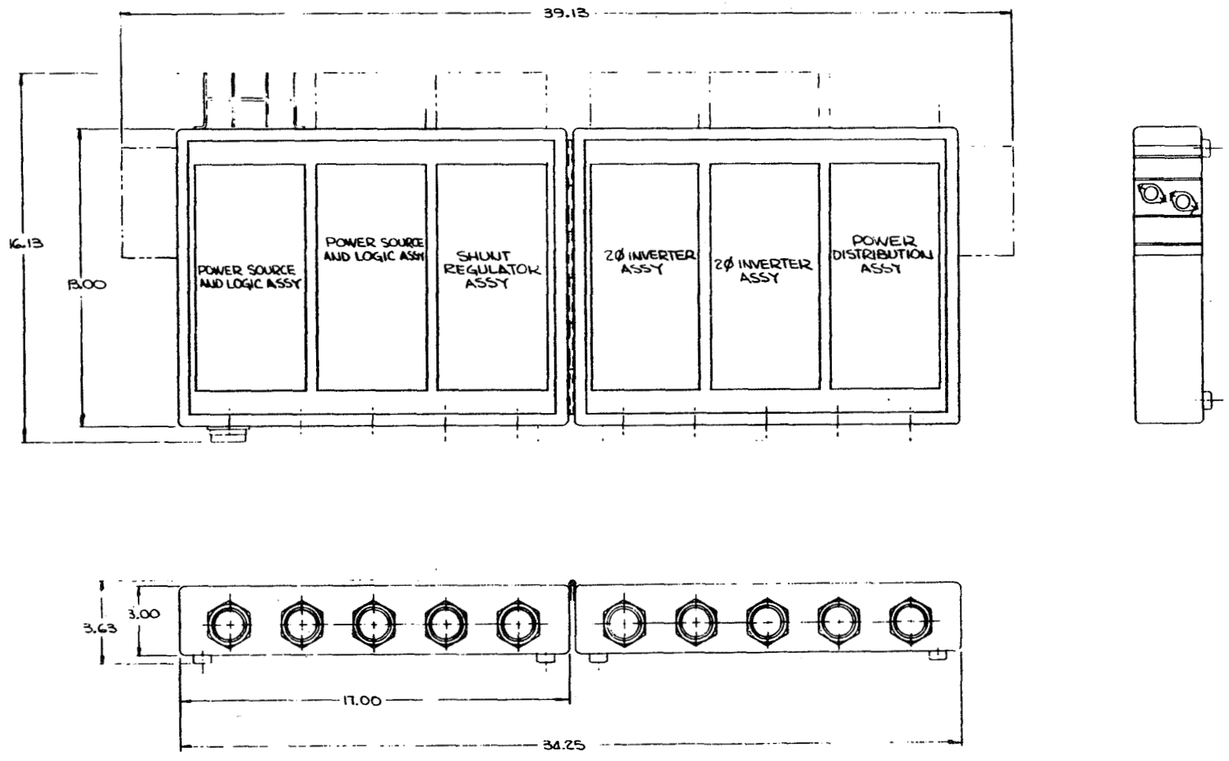


Figure 6-1. Breadboard Packaging Configuration

TECHNICAL DISCUSSION

SECTION 7. ANALYSIS

7.1 Operating Frequency Analysis

Introduction

Efficient power processing from a single DC source voltage to multiple user DC voltages is accomplished by DC to DC converters. These generally use transistor switches to produce a square wave that is transformed, rectified, and filtered to obtain the desired output voltages. The peculiar effects of the inversion frequency on each function of the conversion process suggests the frequency of operation. Weight of power conditioning equipment is generally reduced as frequency increases, but the resulting inefficiencies in magnetics and semiconductors increase heat sink requirements and primary power source weight. Therefore, total system weight can be minimized by varying the inversion frequency, and there is a range of frequencies where minimum weight prevails. The objective of this study is to identify this frequency range. Selection of a discrete frequency within this range may then be based on other system criteria.

Approach

Figure 7-1 is a functional block diagram of a DC to DC converter. The principal functions that are affected by frequency are the transformer and the transistor switches. These were analyzed and reported in the "Final Report - Mars Spacecraft Power System Development", JPL Contract 952150, performed by the General Electric Company, and reproduced here in part for continuity. A similar approach was used in this study, and secondary effects of filter weight, rectifier efficiency, and source and heat sink penalty for lower efficiency were also considered. The primary approach was to review an AC distribution system, to vary the number of loads, and then to apply the results to a decentralized DC system.

Technical Discussion

Table 7-1 is a summary of assumptions and input variables considered for this study. The source and heat sink weight penalty for inefficiencies is considered along with the transformer and filter weight. The power level of 200 watts was assumed since this level changes only the relative magnitude of the weight and does not affect frequency. Power conditioning weight is primarily determined by the magnetic components -- the inductor and transformer. These may be designed for a constant efficiency regardless of frequency. Power conditioning efficiency is determined by individual efficiencies of each function shown in the block diagram of Figure 7-1. Only the transistor switch and the rectifier efficiency are frequency dependent, and are examined accordingly. Each element of the converter is considered separately below.

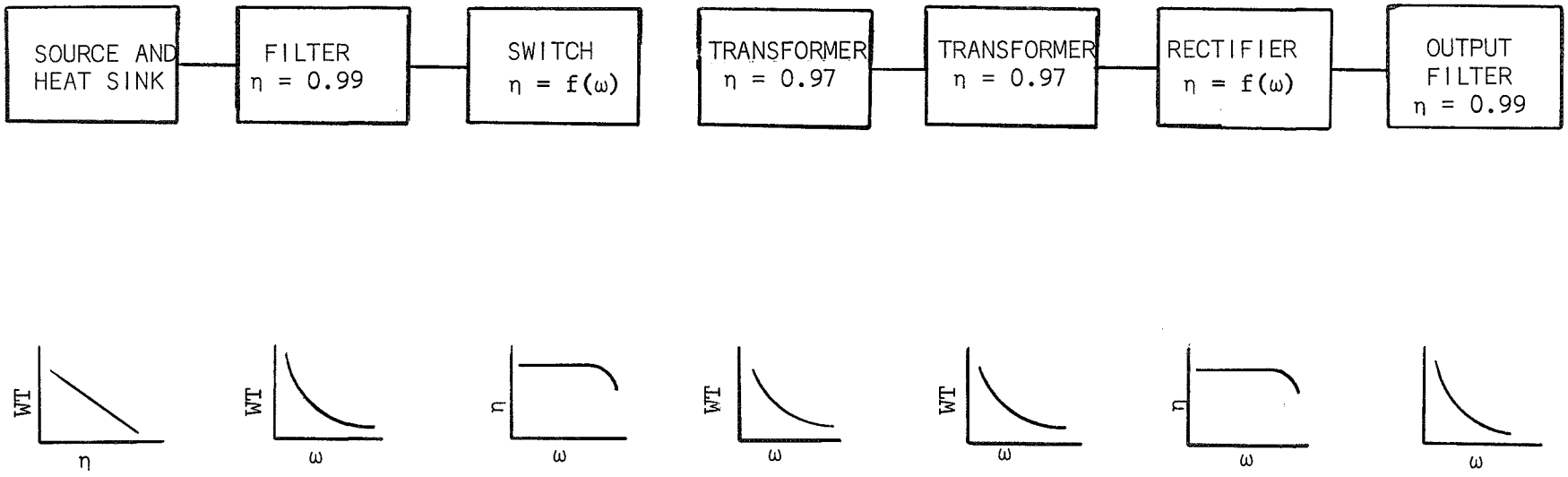


Figure 7-1. DC-DC Process Functional Block Diagram

TABLE 7-1. Assumptions and Input Variables

	ASSUMED CONSTANT	INPUT VARIABLE
FILTER	• EFFICIENCY - 98 PERCENT	• WEIGHT (FREQUENCY DEPENDENT)
TRANSFORMER	• INPUT - OUTPUT ISOLATION • $V_{OUT} = V_{IN}$ • EFFICIENCY - 97 PERCENT	• WEIGHT (FREQUENCY DEPENDENT)
TRANSISTOR POWER SWITCH	• WEIGHT	• EFFICIENCY (FREQUENCY AND SWITCH SPEED DEPENDENT) • INPUT VOLTAGE
RECTIFIER	• WEIGHT	• EFFICIENCY (FREQUENCY AND SWITCH SPEED DEPENDENT)
POWER	• 200 WATTS	
SOURCE	• CAPABILITY 1.2 WATTS PER POUND	
HEAT SINK	• PENALTY 0.07 POUNDS PER WATT	
FREQUENCY		• 400 - 15,000 Hz

Transformer Weight

Transformer size depends on power output, efficiency, temperature rise, voltage level, and frequency. All but frequency are assumed constant. Specific designs were analyzed and the results are plotted in Figure 7-2. Curve 1 is the transformer weight characteristic from the Mars Spacecraft Power System Development Final Report. These designs are based on square wave input voltage. Practically, a finite period occurs during the switching internal during which no power is transferred to the secondary load. In order to maintain the same average current, the peak current must accordingly increase; resulting in additional copper losses as the switching rise and fall times increase. To maintain a constant efficiency, a switch time correction requires additional weight to decrease copper losses. Curve 2 of Figure 7-2 applies a slight switch time correction (k) for storage time (t_s) and fall time (t_f) equal to one microsecond. The dependence on frequency (ω) of this factor is

$$(7\text{-}1) \qquad k = \frac{8\omega(t_s + t_f) - 16\omega^2(t_s + t_f)^2}{1 - 8\omega(t_s + t_f) + 16\omega^2 (t_s + t_f)^2}$$

and was considered for each weight summary.

Transformer weights for multiple loads for either an AC system having transformer rectifiers or a DC system having DC to DC converters were arrived at by using the relation

$$(7\text{-}2) \qquad WT = WT_{OLD} \quad (P_{NEW}/P_{OLD})^{2/3}$$

The total two hundred watts of power was subdivided equally among the ten or twenty loads of the cases considered.

Filter Weight

Filters minimize noise reflected to the power source and to the load. Single inductor and capacitor filters are considered. The design criteria for the inductor is to support the source voltage for one half cycle of the inversion frequency. The current during that period may rise from zero to full load current. The capacitor weight is assumed constant, since it provides energy only during the switching interval; and this is relatively constant regardless of frequency.

Figure 7-3 is a filter weight summary as a function of frequency. This curve represents the total input and output filter weights for either an AC system or a DC system. This is based on equivalent load and source requirements and the assumption that the attenuation of generated noise is comparable for either system. Therefore, this curve was applied to the weight analysis along with the switch time correction derived for the transformer.

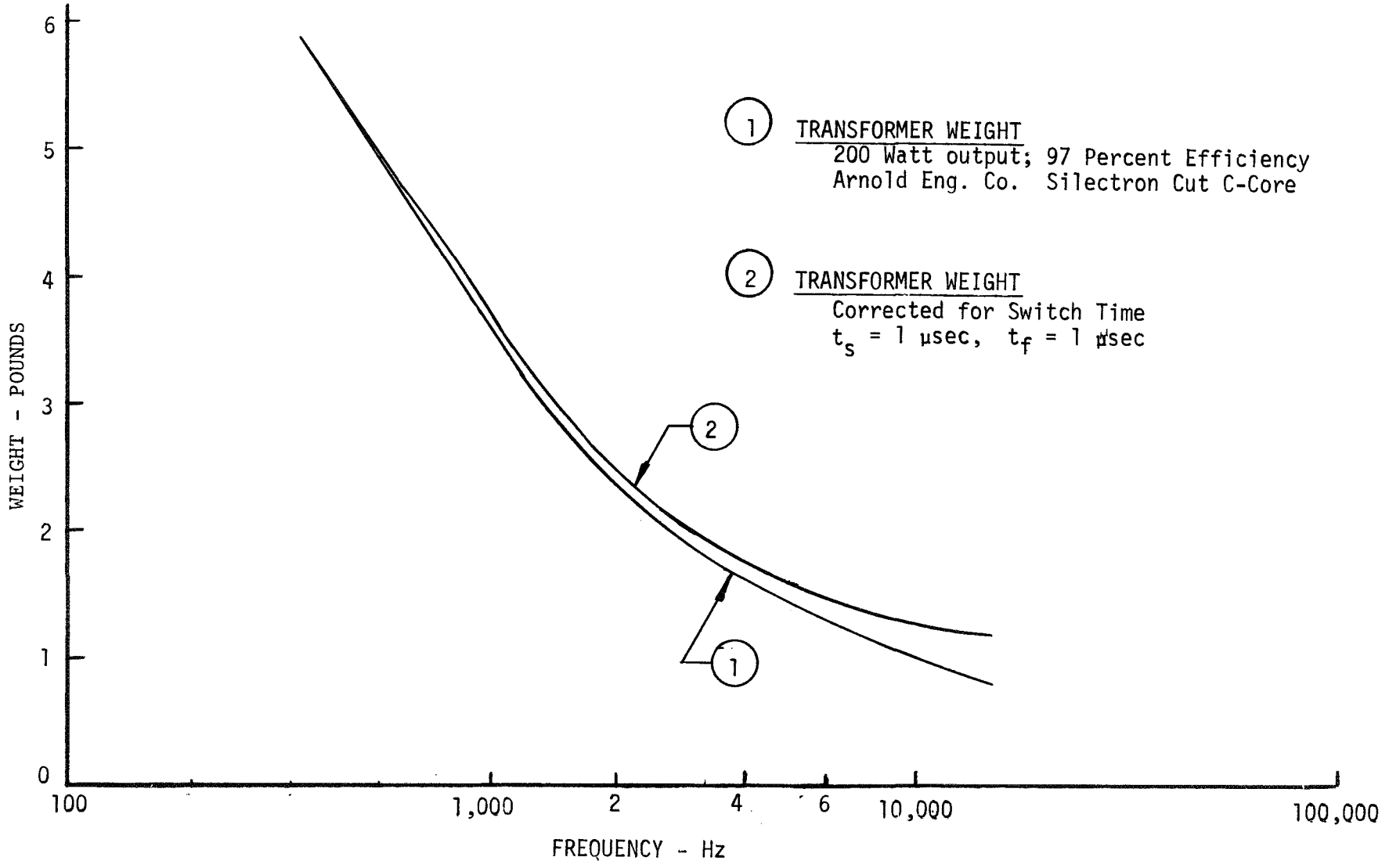


Figure 7-2. Transformer Weight

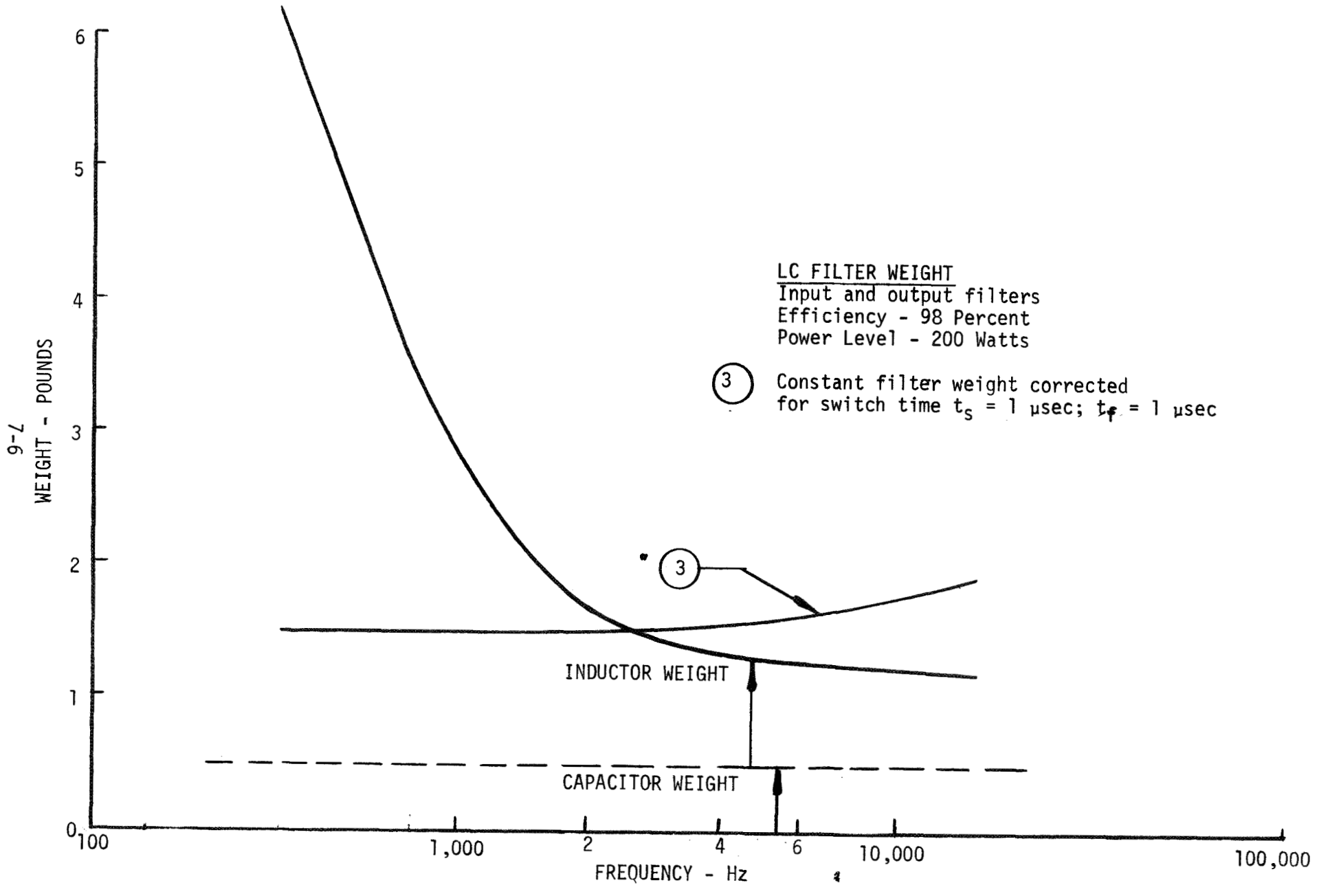


Figure 7-3. LC Filter Weight

A second approach could be considered for weight analysis. The filter requirements are to supply energy only during the switch period. The filter design would be constant and by applying the switch time period correction (k), the filter weight would increase as a function of frequency.

The first approach results in greater weight for the lower frequencies. The second approach presents either constant weight or a greater weight at higher frequencies only if the switch period becomes significant. Curve 3 of Figure 7-3 shows the filter weight for t_s and t_f equal to one microsecond. (One microsecond is not considered significant.) A review of both approaches was performed.

Inverter Efficiency

Inverter efficiency is affected by transistor and transformer losses. The transformer losses are relatively constant over a wide range of frequency. The transistor and diode losses, on the other hand, are sensitive to frequency and are accordingly treated below.

The inverter efficiency (η) as a function of output power (P_o) is

$$\eta = \frac{P_o}{P_o + \text{Transformer loss} + \text{Transistor loss}} \tag{7-3}$$

with a 95 percent efficient transformer, and to a first order effect,

$$\eta = \frac{P_o}{P_o + (0.05)\ P_o + \text{Transistor loss}} \tag{7-4}$$

or, simplifying,

$$\eta = \frac{1}{1.05 + \frac{\text{transistor loss}}{P_o}} \tag{7-5}$$

Transistor Loss

The power switch operates either full on or full off with a finite time required for transfer. This transfer time is determined by intrinsic transistor characteristics and results in switching power losses. The more frequent the switch transfers the greater are the switching losses. These characteristics are altered by drive control and load. Drive control is primarily determined by load current magnitude, and it affects switching losses only if insufficient reverse bias is provided during the switch OFF time. Assuming that drive control conditions are adequate, load is the only remaining parameter to affect the intrinsic characteristics of the transistor switch. Part of the real load is the power transformer, and it is examined along with load to establish the conditions during switch transfer from ON to OFF.

The equivalent circuit seen by the transistor switch is shown in Figure 7-4. Switches Q1 and Q2 are the power transistors, TXis the ideal transformer, R_L is the nominal load, and the balance is the transformer impedances seen by the power switch. The transformer impedances somewhat distort the desired square wave. Further, the switches are not considered fully open or closed until the transformer is in a stable state. Thus, the transistor switching time is affected by the transformer frequency response.

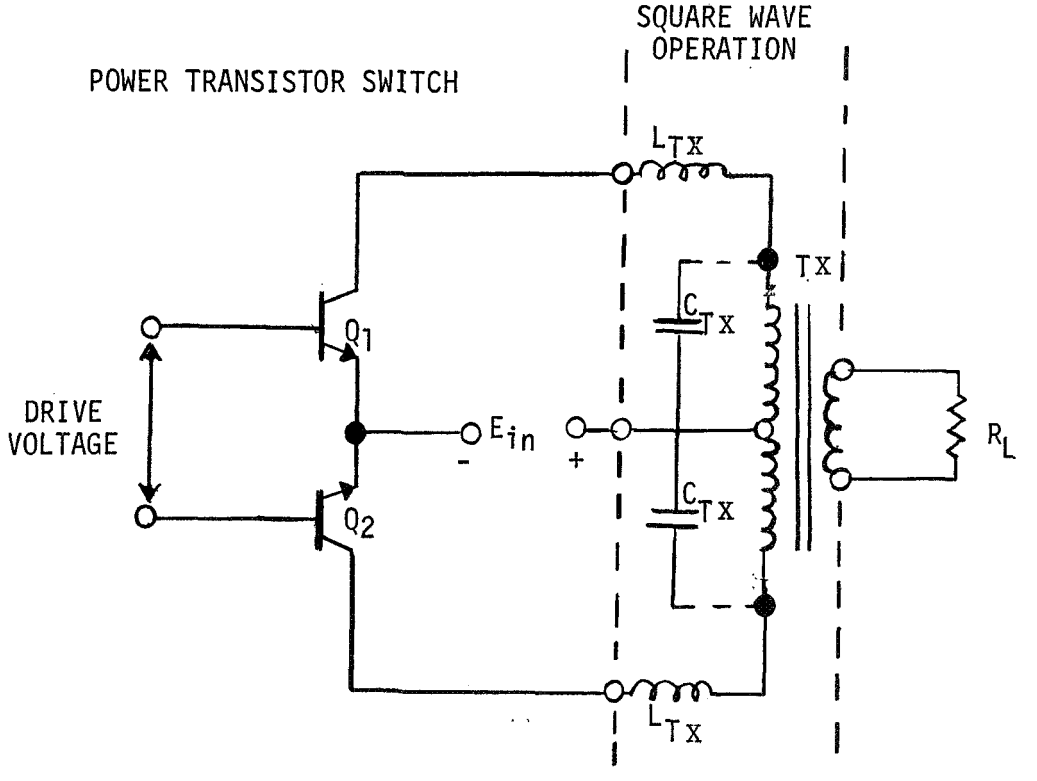


Figure 7-4. Circuit Diagram, Push-Pull Inverter

Since power transformer efficiency is constant by design, the inverter efficiency can be analyzed by considering only power switching losses as a function of frequency. These losses are expressed by the following equation which is derived in the following sections:

$$(7\text{-}6)\quad P_{sw} = \frac{V_{in}I_c}{T}\left[0.71\ t_s + \frac{4}{3}\left(\frac{t_s t_f}{t_s + t_f}\right) + \frac{5}{3}\left(\frac{t_f^2}{t_s + t_f}\right) + 0.33\ t_f\right] \times \left[\frac{1}{1 - \frac{4}{T}(t_s + t_f)}\right]$$

where:

P_{sw} is the power switch loss in watts (P_{sw} occurs twice per cycle)

V_{in} is the supply voltage less $V_{ce\ SAT}$, and

I_c is the peak collector current.

This expression was used in the efficiency calculations.

Transistor Switching Diagrams

The transistor switching diagram for a push-pull configuration is shown in Figure 7-5. The switch forcing function is the drive power shown in time only for Q1 and Q2. Consider that Q1 is ON and the level of collector current $I_{c\ 1}$ is determined by R_L. At time t_1 the drive to Q1 is removed and drive to Q2 is applied. Collector current of Q1 continues to flow due to load effects and transistor storage time, t_s. Transistor Q2 starts to turn on denoted by the fall of V_{ce_2} and rise of I_{c2}. Since Q1 is still on and Q2 is turning on, the high impedance normally presented by the transformer is reduced such that I_c of Q2 rises to a level determined by transistor drive current and gain. For this analysis a gain limit of two times that required is assumed. Therefore, I_{c2} rises to $2I_{c2}$ until Q1 begins to open such that the impedance presented by the transformer increases, reducing I_{c2} to a level determined by R_L. Thus, the diagram shows the relation between rise, fall and storage time of a transistor. Note that the rise time, t_r, is a function of t_s and t_f. The switching diagram associated with the time diagram is Figure 7-6. The power dissipated during the switching period is then the summation of each period of t_r, t_s, t_f; where t_r is determined by t_s and t_f.

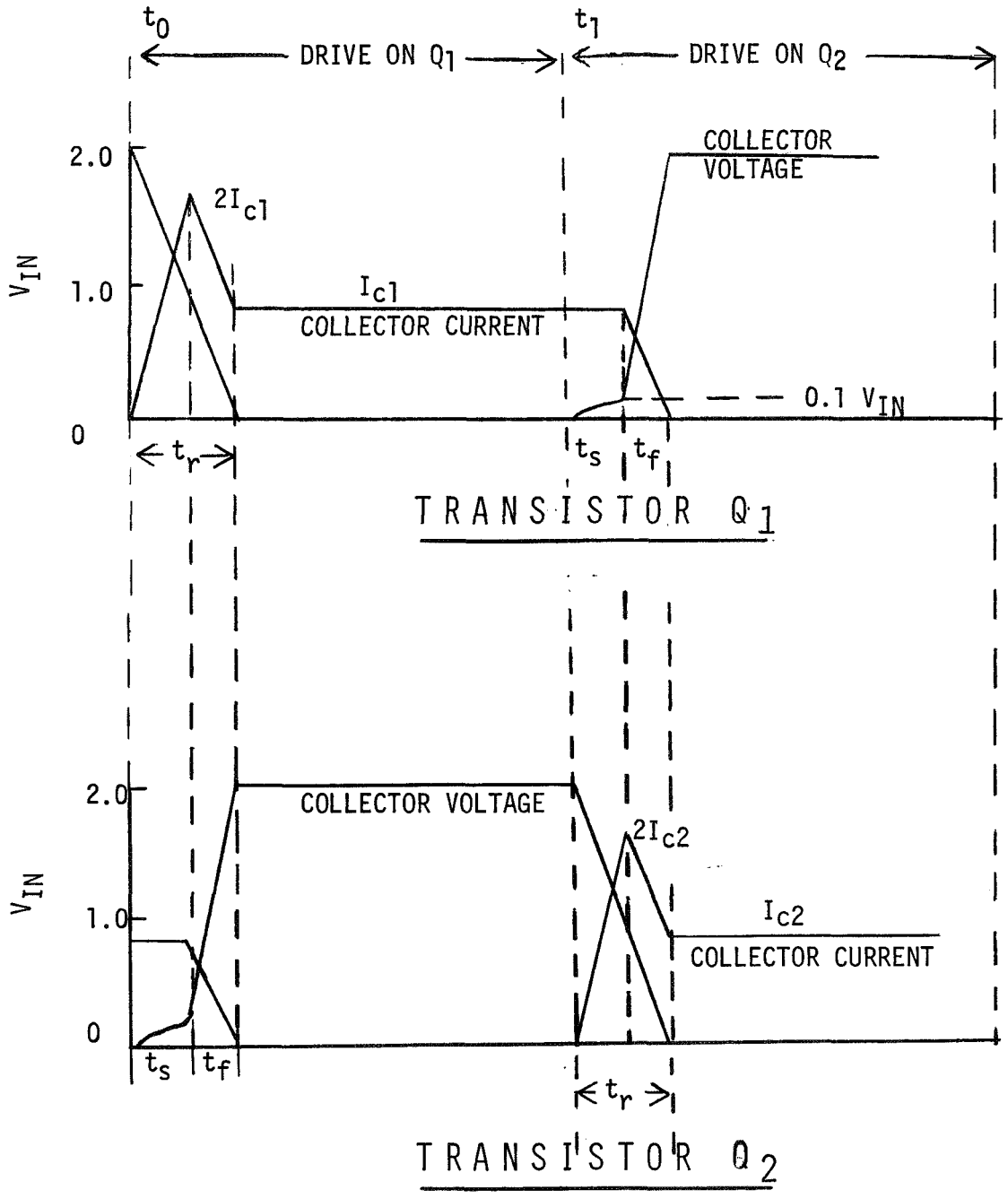
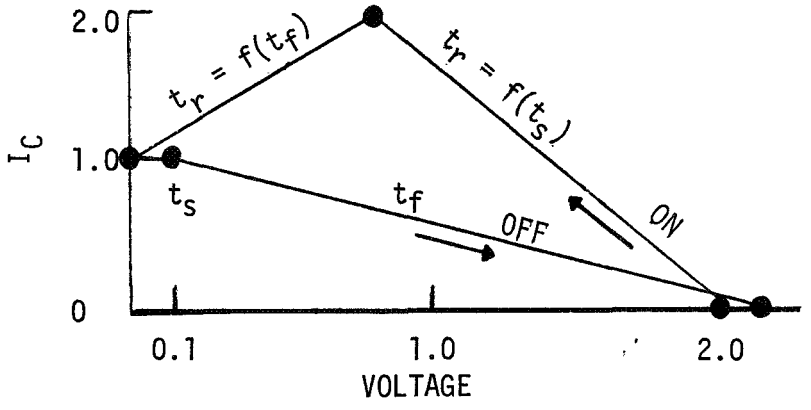
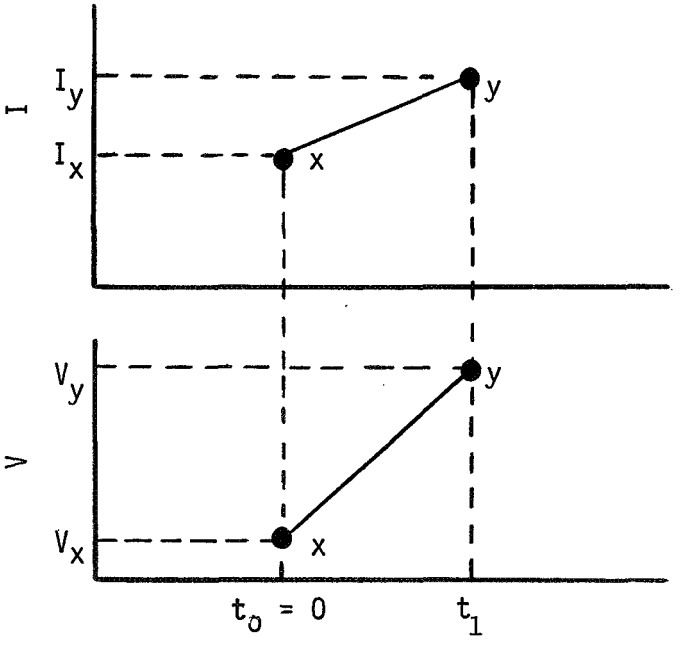


Figure 7-5. Switch Voltage-Current-Time Diagram of Push-Pull Inverter



$$V_{ce} = 1.0 \cong E_{in}$$

Figure 7-6. Switching Diagram



$$i = I_x + \frac{I_y - I_x}{t_1} t$$

$$v = V_x + \frac{V_y - V_x}{t_1} t$$

Figure 7-7. Linear Switching

Power Dissipation General Case

Since the voltage-current for each time period of the diagram can be considered linear, a general case power dissipation for each time period may be derived. Consider the general case for linear switching shown in Figure 7-7. The instantaneous current is

$$(7\text{-}7) \quad i = I_x + \left(\frac{I_y - I_x}{t_1} \right) t,$$

and the instantaneous voltage is

$$(7\text{-}8) \quad v = V_x + \left(\frac{V_y - V_x}{t_1} \right) t.$$

The power for this interval is

$$(7\text{-}9) \quad P = \frac{1}{T} \int_0^{t_1} v\, i\, dt\ ,$$

where T is the period of inversion.

This equation reduces to

$$(7\text{-}10) \quad P = \frac{t_1}{6T} \left[(V_x I_y + V_y I_x) + 2(V_y I_y + V_x I_x) \right]$$

Thus each interval is examined using this equation, and the total switching loss is a summation of each interval during T, the period of one cycle of inversion.

Derivation of Transistor Switch Loss

The general equation for linear switching is

$$(7\text{-}11) \quad P = [t/6T][(V_x I_y + V_y I_x) + 2(V_y I_y + V_x I_x)]$$

Referring to Figure 7-5, at Q2 turn on the rise time, t_r, is shown in two parts. The first is shown related to storage time, t_s, and the second is shown related to fall time, t_f. Power loss (P_r) during this time period is the sum of the losses during the two intervals.

Since V_{ce} nearly equals $2V_{in}$ when the transistor is off, V_{in} is used for clarity because V_{ce} appears later when the transistor is on. For the switching period calculations, the transistor $V_{ce_{SAT}}$ is considered negligible since the error is much less than one percent.

The power loss during the rise time is as follows:

During t_s

$$(7\text{-}12) \quad P_r = [t_s/6T]\left[(2V_{in} \cdot 2I_c + 0) + 2\left(2V_{in}\left(1 - \frac{t_s}{t_s+t_f}\right)2I_c + 0\right)\right]$$

$$(7\text{-}13) \quad P_r = \left[\frac{2V_{in}I_c\, t_s}{3T}\right]\left[\frac{t_s + 3t_f}{t_s + t_f}\right]$$

During t_f

$$(7\text{-}14) \quad P_r = \frac{t_f}{6T}\left[\left\{2V_{in}\left(\frac{t_f}{t_s + t_f}\right)I_{c_2} + 0\right\} + 2\left\{0 + 2V_{in}\left(\frac{t_f}{t_s + t_f}\right)2I_c\right\}\right]$$

$$(7\text{-}15) \quad P_r = \frac{5V_{in}I_c\, t_f^2}{3T(t_s + t_f)}$$

and during $t_s + t_f$,

$$(7\text{-}16) \quad P_r = \frac{V_{in}I_c}{3T(t_s + t_f)}\left[2t_s^2 + 6t_s t_f + 5t_f^2\right]$$

The power loss during the storage time is

$$(7\text{-}17) \qquad P_s = \frac{t_s}{6T}\left[(0 + 0.1\ V_{in}\ I_c) + 2(0.1\ V_{in}\ I_c + 0)\right]$$

$$(7\text{-}18) \qquad P_s = \frac{0.1\ V_{in}\ I_c\ t_s}{2T}$$

The power loss during the fall time is

$$(7\text{-}19) \qquad P_f = \frac{t_f}{6T}\left[(0 + 2\ V_{in}\ I_c) + 2(0 + 0.1\ V_{in}\ I_c)\right]$$

$$(7\text{-}20) \qquad P_f = \frac{2.2\ V_{in}\ I_c\ t_f}{6T}$$

The total switch losses (P_{sw}) are

$$(7\text{-}21) \qquad P_{sw} = \left[\frac{V_{in}\ I_c}{6T}\right]\left[\frac{4t_s^2 + 12t_s t_f + 10t_f^2}{(t_s + t_f)} + 0.3t_s + 2.2t_f\right]$$

This power loss due to switching is described by T, V_{in}, I_c, t_s, and t_f; and occurs twice per period.

Note that if frequency increases, the percent time that the transistor is ON becomes less. Therefore, in order to supply the same average load current the peak collector current I_c must increase as frequency increases. The derived factor (from next paragraph) for this is,

$$\left[\frac{1}{1 - \frac{4}{T}(t_s + t_f)}\right]$$

Total Transistor Losses

Transistor losses are

$$(7\text{-}22) \qquad P_{tot} = 2P_{sw} + P_{dr} + P_{sat}$$

where:

P_{sw} = Equation 7-21

P_{dr} = 0.025 P_o , and

P_{sat} = $V_{ce\ SAT}$ I_c where P_{sw} , P_{drive}, P_{SAT} are corrected by multiplying by the collector current correction factor since all are related to I_c.

Collector Current Frequency Correction

In terms of transistor efficiency as a function of frequency where the average current is a constant and the percent of ON time decreases due to fixed switch time and shorter ON time, I_c increases as a function of frequency to maintain the average current.

(7-23) I_{AVE} = K_A = Constant per load requirements

(7-24) I_{AVE} = I_c at frequency equal to zero

then I_{AVE} = K_f I_c at frequency greater than zero, where K_f is a factor which changes as a function of frequency causing I_c also to change in order to maintain a constant I_{AVE} . The factor K_f is determined by reference to Figure 7-8 and the following text.

For simplicity it is assumed that no power is delivered to the load during the periods $(t_s + t_f)$.

Then

(7-25) $$I_{AVE} = \frac{(T/2) - 2(t_s + t_f)}{T/2} I_c = K_f I_c$$

where:

(7-26) $$K_f \equiv 1 - \frac{4}{T}(t_s + t_f)$$

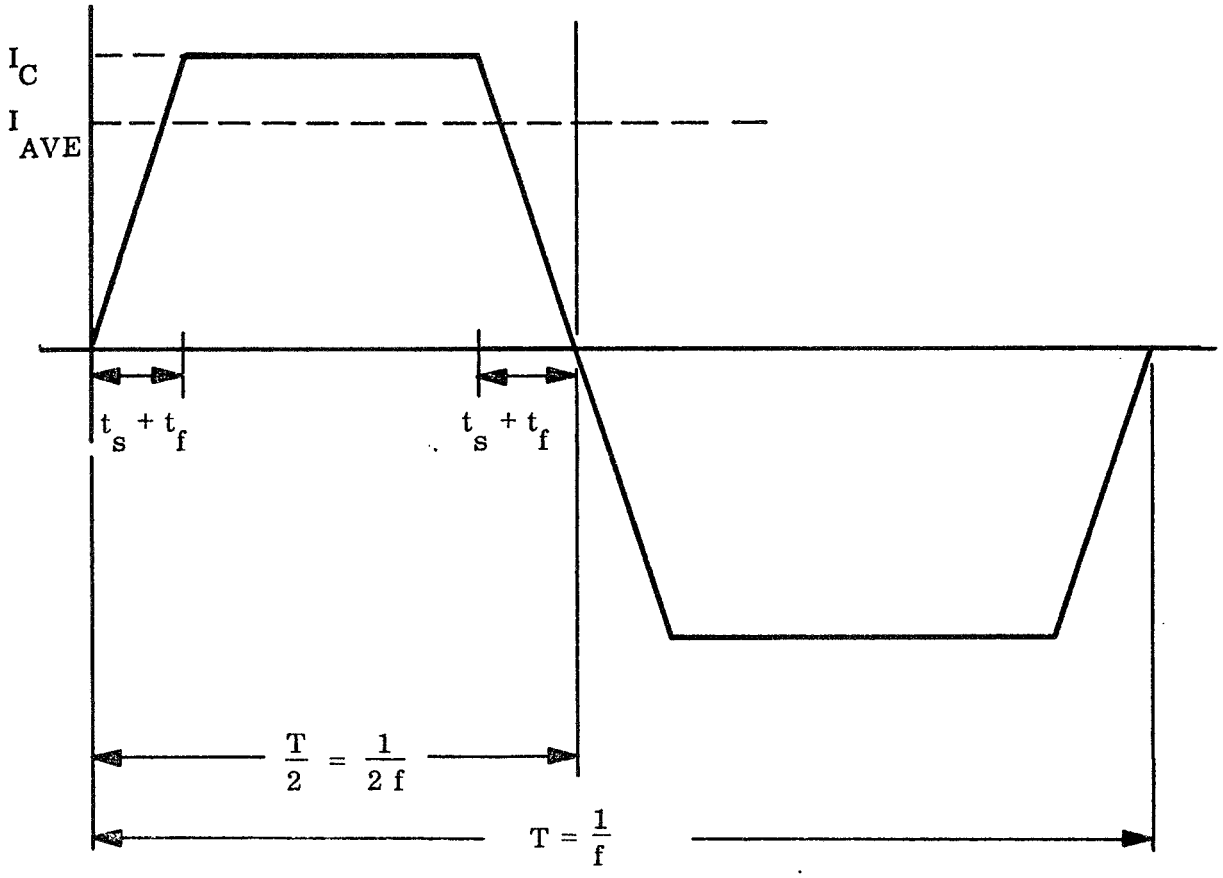


Figure 7-8. Inverter Collector Current-Time Diagram

If K_f decreases as a function of frequency, I_c must increase by the inverse of K_f in order to maintain a constant I_{AVE}. Thus, I_c is corrected for frequency by the term

$$\left[\frac{1}{1 - \frac{4}{T}\ (t_s + t_f)}\right]$$

Note that if the peak I_c increases then the base drive must corespondingly increase, and the base drive must also be adjusted by the same factor. Note also that saturation losses increase also and are adjusted accordingly.

Rectifier Losses

Rectifier loss is treated similarly to the transistor switch loss as a function of frequency. The losses are expressed by the following equation, which is derived in the following sections.

$$(7\text{-}27) \quad P_{rsw} = \frac{V_R\ I_D}{T}\left[1/6\ t_{rec}\right]$$

where

P_{rsw} is power rectifier switching loss in watts

V_R is peak reverse voltage seen by rectifier

I_D is rectifier peak current

t_{rec} is recovery time of diode

P_{rsw} occurs twice per cycle.

Using the general equation for linear switching derived previously, the diode rise and fall time losses are derived with reference to Figures 7-9 and 7-10 as follows:

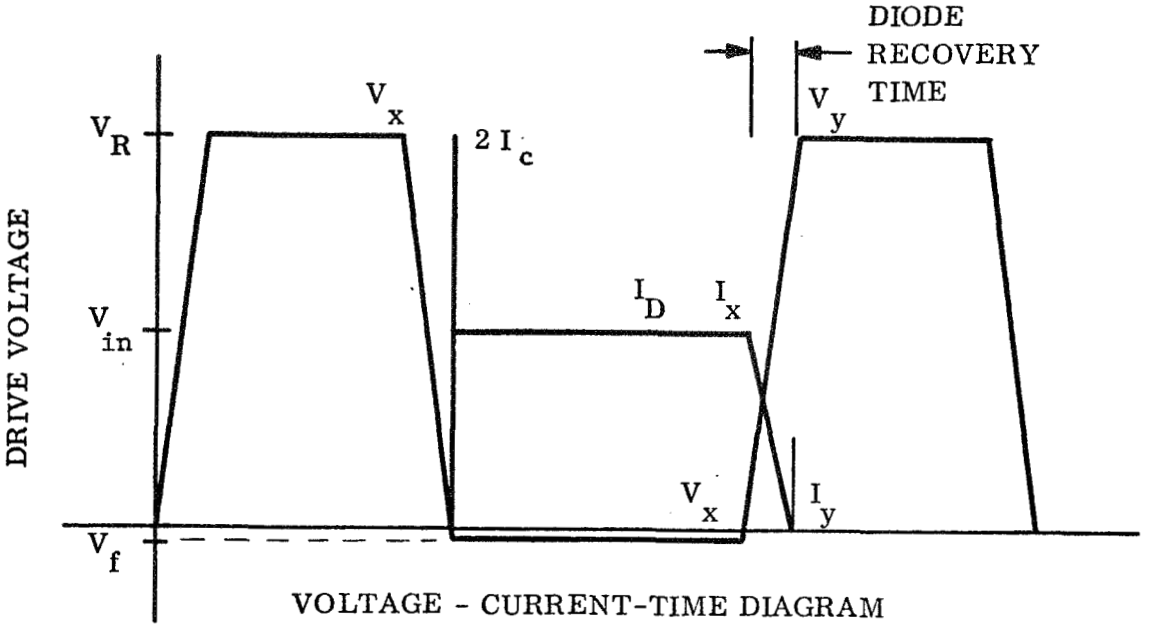


Figure 7-9. Full Wave Rectifier/Choke Input Filter

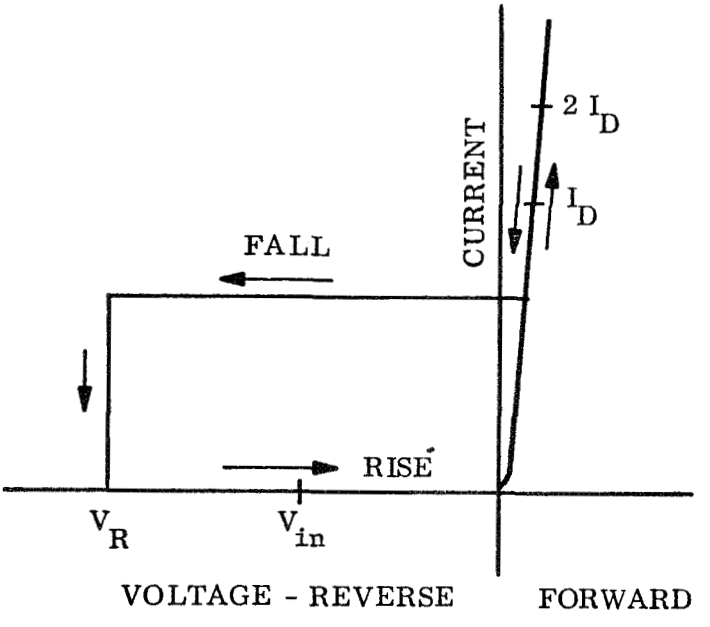


Figure 7-10. Rectifier Switching Characteristics

The rectifier voltage-current curve shows that very little power is lost in the diode during the rise time. The primary power loss is during the fall time, which is the diode recovery time.

(7-28) $$P = (t/6T)\left[(V_x I_y + V_y I_x) + 2(V_y I_y + V_x I_x)\right]$$

(7-29) $$P_f = (t/6T)\left[(0 + V_R I_D) + 2(0 + 0)\right]$$

(7-30) $$P_f = \frac{V_R I_D t_{rec}}{6T}$$

where:

P_f is power rectifier fall time switching loss in watts.

V_R is reverse voltage seen by rectifier

I_D is forward current at time of switching off

t_{rec} is recovery time of rectifier.

Total rectifier losses are

(7-31) $$P_{total} = P_{forward} + {}^{2P}{}_{f} ,$$

(7-32) $$P_{total} = V_f I_D + \frac{V_R I_D t_{rec}}{3T},$$

where V_f is the diode forward voltage drop.

Transformer Size Correction

The efficiency of the transformer is determined by core and copper losses. As the switching time increases, the transformer peak currents increase in order to maintain the same average current. For constant efficiency, copper losses are to remain constant, and winding resistances must be reduced to compensate for the increase in peak currents. The required copper increase results in an increase in transformer size.

Figure 7-8 shows the transistor collector current and may also represent transformer current. The collector current correction factor, therefore, may be used for determining the change in transformer size. This is shown below:

$$P_{avg} = I_c^2 R, \tag{7-33}$$

where R is the total equivalent resistance, and

$$I_c = I_{co}\left[K_f\right]. \tag{7-34}$$

If P_{avg} is to remain constant, then R must decrease by the factor that $(I_c)^2$ increases.

$$P_{avg} = \left[I_{c_o}\left(\frac{T}{T - 4(t_s + t_f)}\right)\right]^2 R \tag{7-35}$$

$$R_{new} = (R/T)\left[T - 4(t_s + t_f)\right]^2. \tag{7-36}$$

If R were known, a new resistance (R_{new}) could be calculated. For a general case this approach does not apply, since R is not available. However, if R were assumed constant, the efficiency change could be determined and a size correction could be made based on the necessary efficiency increase and the relation of efficiency to weight. In the region of transformer efficiencies of 97 to 98 percent, an increase of one percent results in a fifty percent transformer weight increase. In the region of 98 to 99 percent, a one percent increase in efficiency doubles the transformer weight. Figure 7-11 is a plot of these characteristics. The change in power loss is the correction factor (K_t),

$$K_t = \frac{P_2 - P_1}{P_1} \tag{7-37}$$

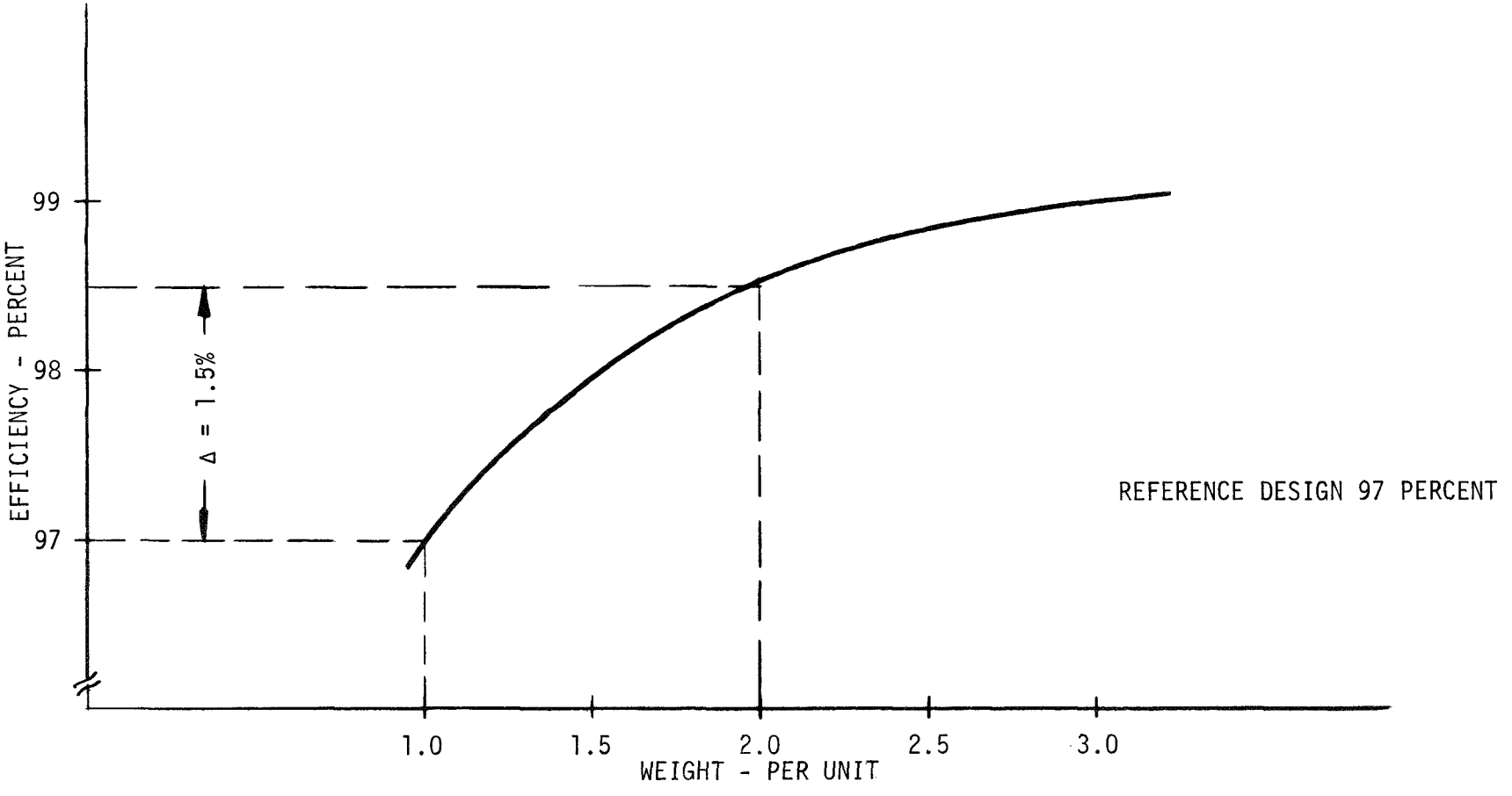


Figure 7-11. Transformer Efficiency - Weight

where

(7-38) $P_1 = I_c^2 R$ at $\omega = 0$,

(7-39) $P_2 = I_c^2 R$ at $\omega > 0$,

(7-40) $P_2 = I_c^2 K_f^2 R$, and

$K_t = 1.0$ represents a transformer efficiency change of 1.5 percent.

The term $I_c^2 R$ is cancelled from each term.

(7-41) $$K_t = \frac{(K_f)^2 - 1}{1} = \left(\frac{T}{T - 4(t_s + t_f)}\right)^2 - 1$$

(7-42) $$K_t = \frac{8T(t_s + t_f) - 16(t_s + t_f)^2}{1 - 8T(t_s + t_f) + 16(t_s + t_f)^2}$$

The factor K_t may be used to determine the increase in transformer weight where $K_t = 1.0$ represents a required weight increase of approximately 100 percent. A straight line assumption for K_t was used between 97 and 98.5 percent.

This factor may also be applied to inductors that are required to conduct pulses of current.

Efficiency Calculations

The loss expressions derived for transistors and rectifiers were used in a computer program to determine power conditioning efficiencies as a function of frequency. The expression for K_t was also programmed for application to transformer weight data. The program inputs are:

t_s - transistor storage time,

t_f - transistor fall time,

t_{rec} - rectifier recovery time,

V_{in} - Power conditioner input voltage,

V_f - rectifier forward voltage drop,

EFO - initial power conditioning unit efficiency,

PL - output power requirement

F - frequency, 400 to 15000 Hertz.

The program outputs are:

P_{dr} - transistor drive power

P_{do} - rectifier loss,

P_{sw} - transistor switch loss,

P_{sat} - transistor saturation loss,

P_{tr} - total transistor loss,

P_{tot} - total loss,

EFF - power processing efficiency,

WT - source weight penalty for inefficiency,

K_f - collector current correction,

K_t - transformer weight correction.

Typical print outs are shown in Table 7-2 and 7-3; and a copy of the program is shown in Table 7-4.

Power Processing Efficiency

The effects of frequency on power conditioning efficiency are shown in Figures 7-12 and 7-13. Figure 7-12 shows curves for inverters operating at different input voltages with very fast switch characteristics. The efficiency for power conditioning equipment operating within an input voltage range of twenty to thirty volts results in approximately 1.5 percent efficiency difference. This indicates that a source voltage around thirty volts would provide highly efficient power processing equipment without greatly sacrificing power margin.

Figure 7-13 shows curves for different transistor switch characteristics operating from the same input voltage. Due to the sensitivity of efficiency to transistor switch characteristics switch requirements should be specified. Switch response is also controlled by external circuits; therefore, actual circuits should be used to verify transistor responses. Curve (3, 1, .2) is a probable efficiency characteristic. This curve follows the (3, 3, .2) curve more closely than the (1, 1, .2) curves, indicating that improvements on storage time (t_s) is the more significant parameter for improving efficiency.

System Weight

The effects of frequency on system weight is summarized by the curves of Figure 7-14. The weight shown is the weight of transformers, filters, and the source and heat sink weight for inefficiencies only. A power inverter is considered. This component is described by a single load curve. Since multiple loads are necessary, curves are shown for ten loads and twenty loads. Also shown with these curves is the associated transistor switch responses.

Table 7-2. Switch Losses and Inverter Efficiency
Frequency Response Printout

```
 TS TF TR VIN VCE VF EFO PL =3 1 .2 30 .5 .8 .9 200

   F        PDR      PDO      PSW      PSAT      PTR      PTOT     EFF      WT

EFF= 8.9035007E-01 {KT =  1.2923937E-02 {Kφ =  1.0064412E+00
   400.   5.032   5.378   0.226    3.768   9.252   14.631   0.890   19.74

     8.8694316E-01    3.2784718E-02    1.0162602E+00
  1000.   5.081   5.447   0.573    3.819  10.046   15.494   0.887   20.35

     8.8112324E-01    6.7208523E-02    1.0330579E+00
  2000.   5.165   5.565   1.172    3.908  11.418   16.983   0.881   21.40

     8.7814465E-01    8.5069443E-02    1.0416667E+00
  2500.   5.208   5.625   1.483    3.954  12.128   17.753   0.878   21.93

     8.7511887E-01    1.0338253E-01    1.0504202E+00
  3000.   5.252   5.686   1.800    4.001  12.854   18.540   0.875   22.48

     8.7204473E-01    1.2216317E-01    1.0593220E+00
  3500.   5.297   5.749   2.126    4.049  13.597   19.346   0.872   23.03

     8.6892110E-01    1.4142742E-01    1.0683761E+00
  4000.   5.342   5.812   2.459    4.098  14.359   20.170   0.869   23.59

     8.6574676E-01    1.6119203E-01    1.0775862E+00
  4500.   5.388   5.876   2.801    4.149  15.138   21.014   0.866   24.17

     8.6252046E-01    1.8147448E-01    1.0869565E+00
  5000.   5.435   5.942   3.151    4.201  15.937   21.879   0.863   24.75

     8.5590687E-01    2.2366669E-01    1.1061947E+00
  6000.   5.531   6.077   3.877    4.308  17.594   23.670   0.856   25.94

     8.4199680E-01    3.1512498E-01    1.1467890E+00
  8000.   5.734   6.361   5.448    4.540  21.170   27.531   0.842   28.44

     8.2709505E-01    4.1723355E-01    1.1904762E+00
 10000.   5.952   6.667   7.197    4.798  25.144   31.810   0.827   31.12

     8.1109184E-01    5.3171255E-01    1.2376238E+00
 12000.   6.188   6.997   9.155    5.086  29.584   36.581   0.811   34.00

     7.8474121E-01    7.3130191E-01    1.3157895E+00
 15000.   6.579   7.544  12.575    5.589  37.317   44.861   0.785   38.75
```

Table 7-3. Switch Losses and Inverter Efficiency
Frequency Response Printout

```
TS TF TR VIN VCE VF EFO PL =  1  1  .2 30 .5 .8 .9 200

   F        PDR      PDO      PSW      PSAT      PTR      PTOT     EFF      WT

    8.9157410E-01   6.4308515E-03   1.0032103E+00
  400.  5.016  5.361  0.097  3.751  8.961  14.322  0.892  19.52
 {EFF=          {KT=           {KF=
 {8.9004328E-01 {1.6194068E-02 {1.0080645E+00
 1000.  5.040  5.403  0.245  3.775  9.305  14.708  0.890  19.79

    8.8746083E-01   3.2784718E-02   1.0162602E+00
 2000.  5.081  5.474  0.495  3.817  9.888  15.362  0.887  20.26

    8.8615479E-01   4.1232819E-02   1.0204082E+00
 2500.  5.102  5.510  0.622  3.838  10.134  15.694  0.886  20.49

    8.8483872E-01   4.9785003E-02   1.0245902E+00
 3000.  5.123  5.546  0.750  3.860  10.483  16.030  0.885  20.73

    8.8351251E-01   5.8442987E-02   1.0288066E+00
 3500.  5.144  5.583  0.880  3.882  10.736  16.369  0.884  20.97

    8.8217605E-01   6.7208523E-02   1.0330579E+00
 4000.  5.165  5.620  1.012  3.903  11.092  16.712  0.882  21.21

    8.8082920E-01   7.6083399E-02   1.0373444E+00
 4500.  5.187  5.657  1.145  3.926  11.402  17.059  0.881  21.45

    8.7947186E-01   8.5069443E-02   1.0416667E+00
 5000.  5.208  5.694  1.279  3.948  11.715  17.409  0.879  21.70

    8.7672517E-01   1.0338253E-01   1.0504202E+00
 6000.  5.252  5.770  1.553  3.994  12.351  18.122  0.877  22.19

    8.7110024E-01   1.4142742E-01   1.0683761E+00
 8000.  5.342  5.926  2.119  4.088  13.669  19.595  0.871  23.20

    8.6529279E-01   1.8147448E-01   1.0869565E+00
10000.  5.435  6.087  2.713  4.187  15.049  21.136  0.865  24.25

    8.5929377E-01   2.2366669E-01   1.1061947E+00
12000.  5.531  6.254  3.337  4.291  16.496  22.749  0.859  25.33

    8.4991486E-01   2.9132231E-01   1.1363636E+00
15000.  5.682  6.515  4.332  4.457  18.803  25.318  0.850  27.02
```

Table 7-4. Switch Losses and Inverter Efficiency
Program List

```
10/10/69   16.586

00004 REAL KT
00010 DIMENSION F(14)
00020 1 FORMAT ("SWITCH LOSSES AND INVERTER EFFICIENCY"//)
00030 PRINT 1
00040 DATA F/  400., 1000., 2000., 2500., 3000., 3500., 4000., 4500.,
00050 & 5000., 6000., 8000., 10000., 12000., 15000./
00060 *
00070 2 PRINT:" TS TF TR VIN VCE VF EFO PL "
00080 READ: TS, TF, TR, VIN, VCE, VF, EFO, PL
00090 3 FORMAT ("   F      PDR     PDO      PSW     PSAT     PTR      PTOT
00100 &EFF       WT  "//)
00110 PRINT 3
00120 *
00130 TS=TS/10E5
00140 TF=TF/10E5
00150 TR=TR/10E5
00160 EFF=EFO
00170 *
00180 DO 100  J=1,14
00190 PDR=.025*PL/(1-4*F(J)*(TS+TF))
00200 PDO=(VF*PL/VIN+(2*F(J)*PL*TR)/3)/(1-4*F(J)*(TS+TF))
00205 CF=1/(1-4*F(J)*(TS+TF))
00210 *
00220 DO 10 K=1,4
00230 PSW=F(J)*PL*(.71*TS+.37*TF+(4*(TS*TF)+5*TF**2)/3*(TS+TF))/
00240 &((1-4*F(J)*(TS+TF))*EFF)
00250 PSAT=VCE*PL/(VIN*EFF*(1-4*F(J)*(TS+TF)))
00260 PTR=2*PSW+PSAT+PDR
00270 PTOT=PTR+PDO
00280 EFF=1./(1.05+PTOT/PL)
00285 KT=(8*F(J)*(TS+TF)-16*(F(J)**2)*(TS+TF)**2)/
00286 &(1-8*F(J)*(TS+TF)+16*(F(J)**2)*(TS+TF)**2)
00290 IF(K.EQ.4) PRINT:EFF,KT,CF
00300 10 CONTINUE
00310 *
00320 WT=(1.-EFF)*(.9)*PL
00330 PRINT 90, F(J), PDR, PDO, PSW, PSAT, PTR, PTOT, EFF, WT
00340 100 CONTINUE
00350 *
00360 90 FORMAT (F7.0,3F7.3,F8.3,F7.3,F8.3,F7.3,F7.2//)
00370 GO TO 2
00380 END
```

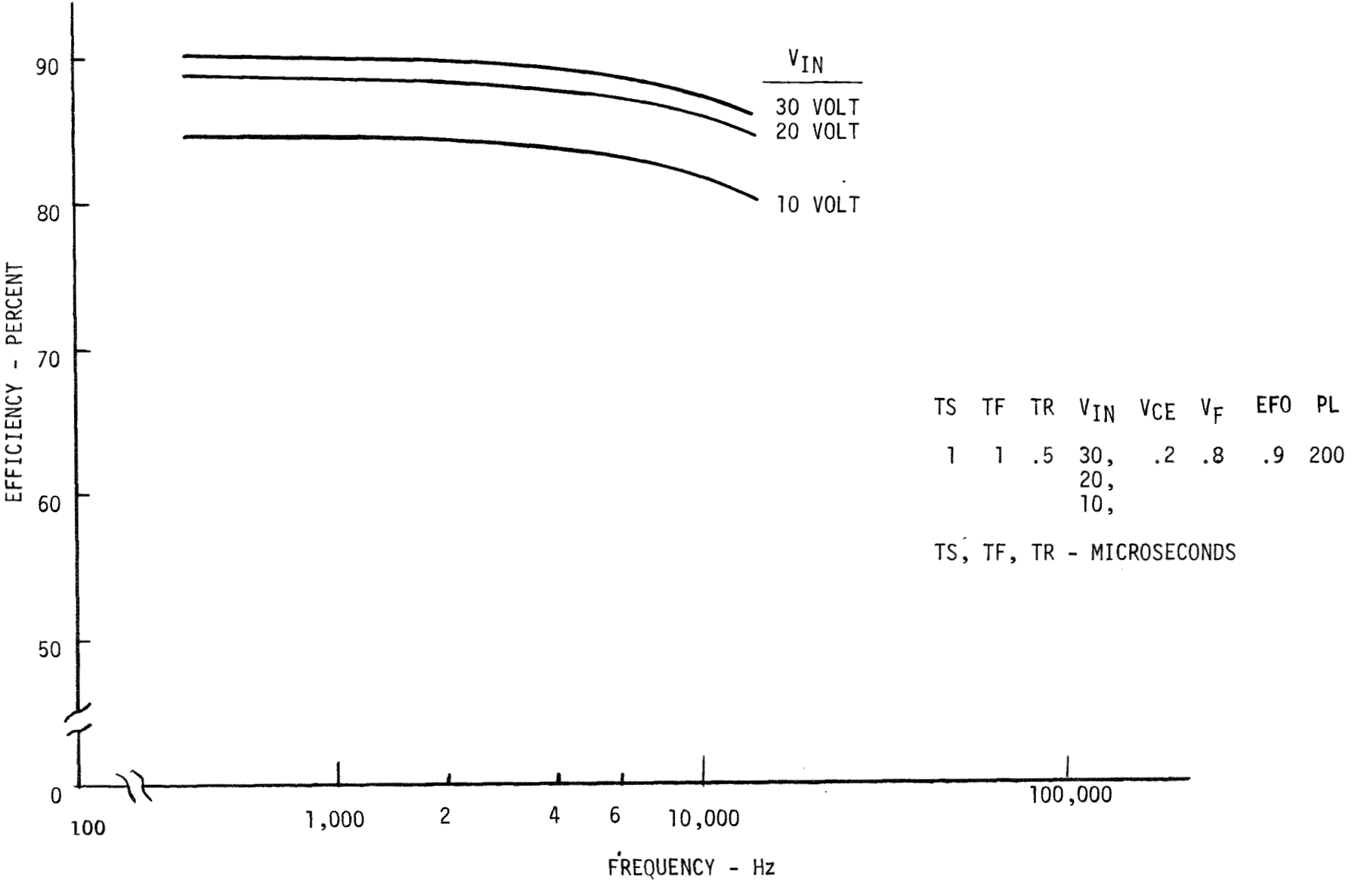


Figure 7-12. Power Processing Efficiency

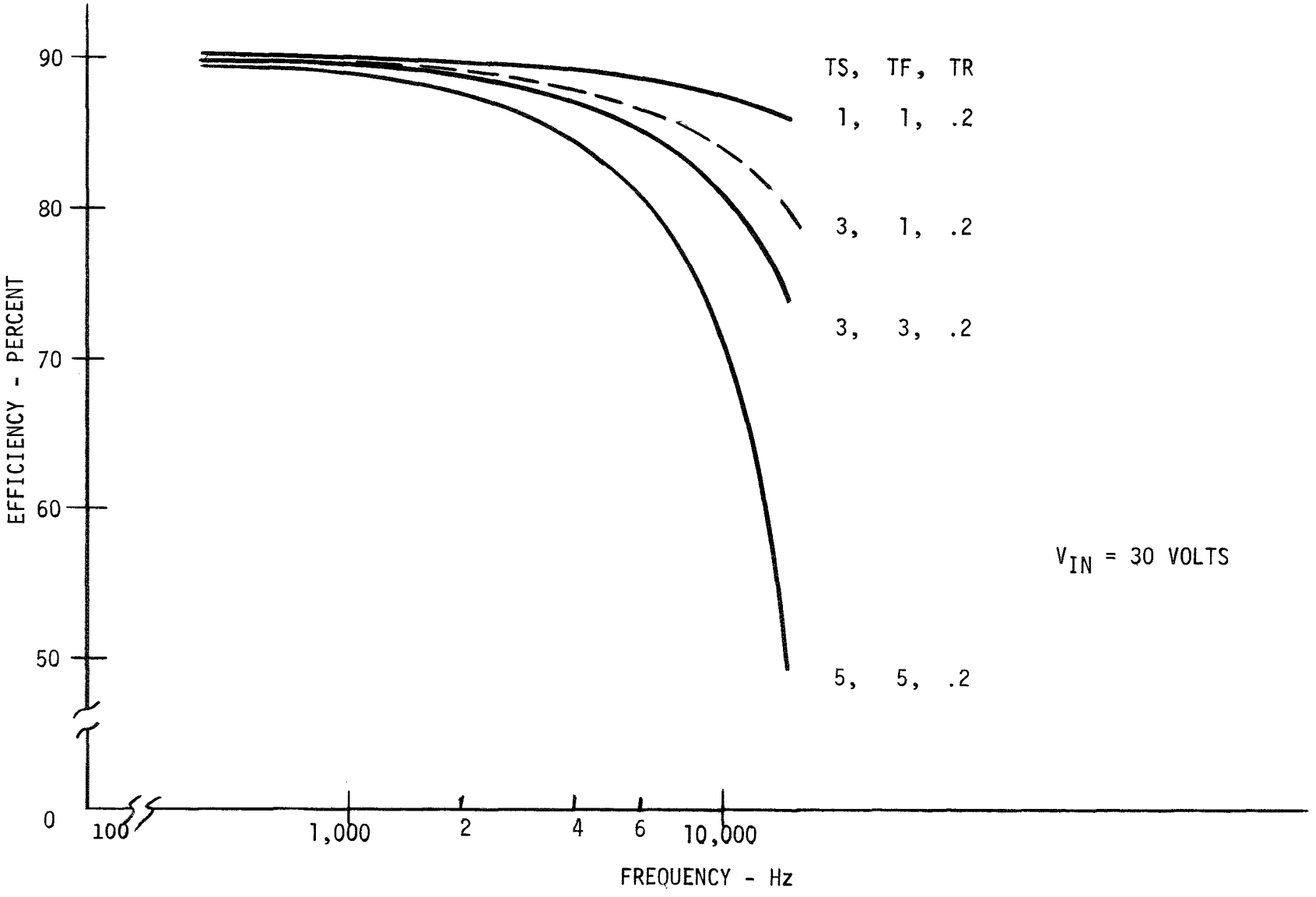


Figure 7-13. 30 Volt Input

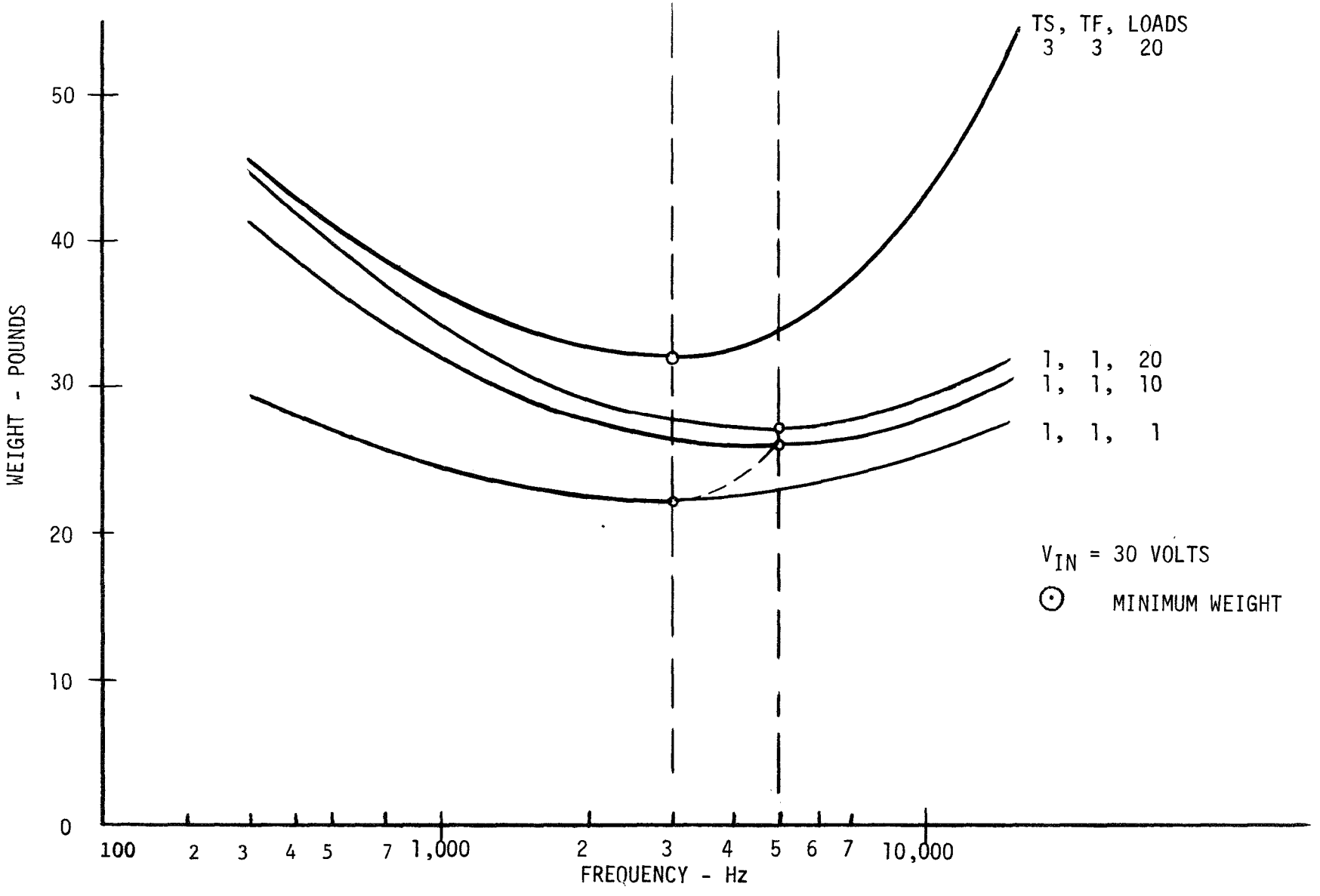


Figure 7-14. Power System Weight

The curve for a single power conditioner is relatively flat. Minimum weight occurs between three and five kilohertz. For more than ten loads, the minimum weight remains at five kilohertz. Therefore, the results presented are applicable to systems having more than ten loads. The greater weight below three kilohertz is the result of filter and transformer weight. The effects of constant filter weight reduce these loads and shift the frequency slightly. A review of Figure 7-3 shows that above three kilohertz filter weight is relatively constant. Transformer weight therefore, has the principal effect. The greater weight above five kilohertz is the result of source and heat sink penalties due to inefficiencies shown in Figure 7-13.

From the weight curves an optimum frequency range is from two to six kilohertz. This range is relatively broad. Examination of the slopes at each frequency provides an indicator of the system weight sensitivity to factors that determine total weight. System weight sensitivity to frequency is shown in Figure 7-15. The data shows that within the present constraints system weight is less sensitive to frequency at the higher end of the usable frequency band.

System weight at the lower end is primarily determined by transformer designs and at the higher end by transistor switch characteristics and source capability. Transformer designs will probably not change in the near future, and therefore the lower end of the curves will not change. Transistor switch responses may be improved by derating and circuit techniques, and the probable response (3,1) may approach (1, 1). Projected source improvements greater than 1.2 watts per pound are expected; therefore, the weight sensitivity to frequency at the higher end will be reduced accordingly. On this basis, the upper end of the range is recommended.

Frequency Recommendations

The usable frequency range where system weight is minimized is from two to six kilohertz. The upper end of the range is recommended.

The analysis included power processing functions for DC to DC conversion. For an AC distribution system a second transformer is added which results in increased weight for lower frequencies and results in a slightly higher lower frequency limit. The weight change within the recommended range, however, is small. The analysis is therefore applicable to both DC and AC systems, when the operating frequency is within the defined usable range. The frequency of operation is not a factor in a comparison of AC and DC distribution systems.

Power subsystem frequency requirements presently require 1600 and 400 Hertz for gyro and momentum wheel power. The recommended frequency for distribution is 4800 Hertz, since it is a multiple of the present system frequency requirements.

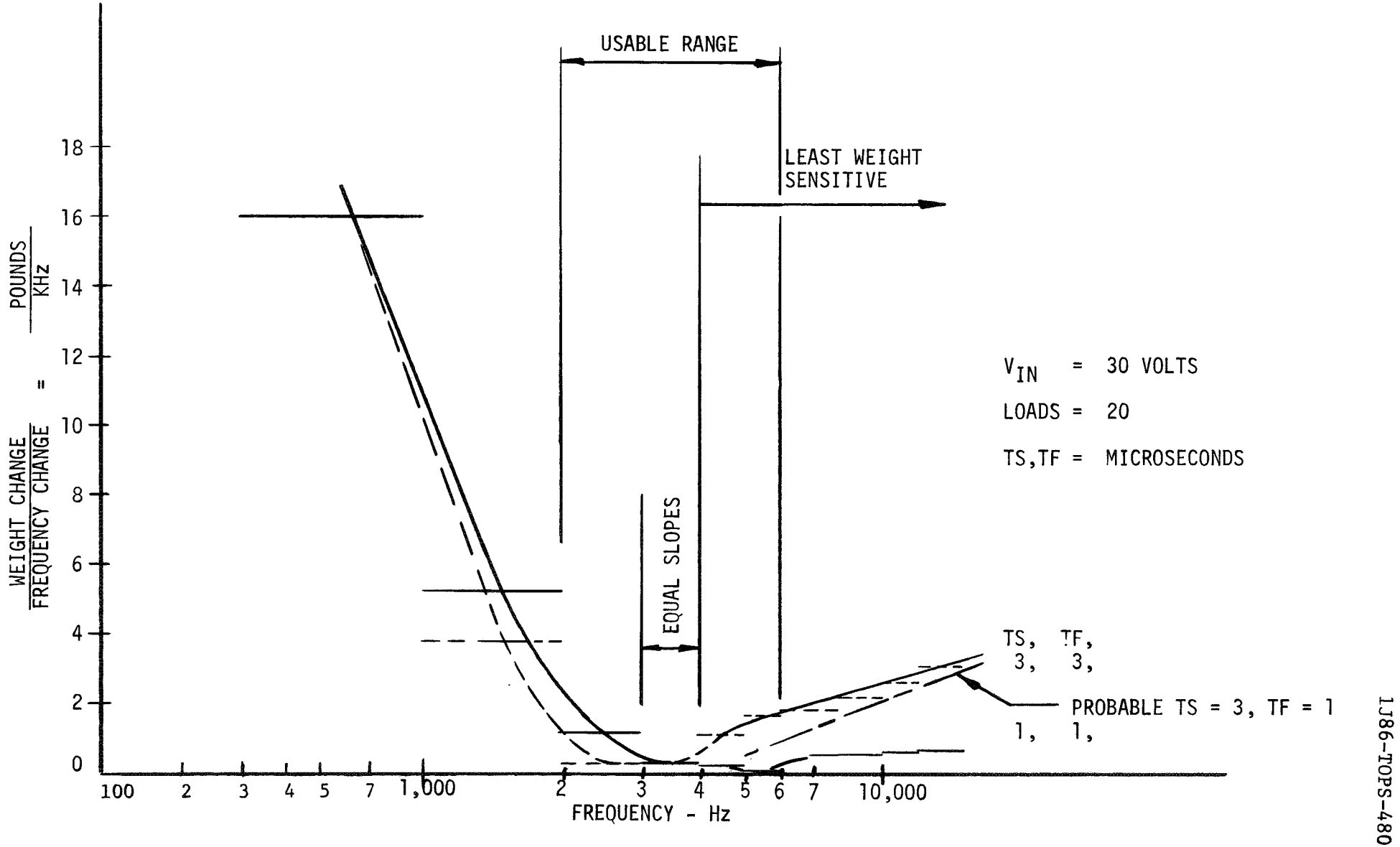


Figure 7-15. System Weight Sensitivity

7.2 Distribution Studies

Introduction

An electrical distribution study was performed to determine the electrical power distribution method for the Thermoelectric Outer Planet Spacecraft. The study objectives were to provide relative comparisons of system performance with respect to power, weight and reliability. Other parameters that were reviewed are thermal control, voltage regulation, size, producibility, electromagnetic interference, and static switching.

Inversion is required because user loads do not use the source voltage directly. Since system performance parameters are sensitive to the inversion frequency, the frequency range was identified where minimum system weight is realized. The primary objectives were to make the selection of the distribution system insensitive to frequency, to select an AC distribution frequency, and to define the frequency range for DC to DC converters for the DC distribution system.

Approach

A review of distribution study parameters generally results in small system differences. This analysis includes those items affected by the distribution system; that is, loads that could be supplied by either AC or DC distribution and that require additional power processing. Loads that use DC power directly at the source voltage, and AC motor loads within the Attitude Control Subsystem, are not considered since they are common to any distribution system.

The power systems considered are shown in Figure 7-16. Each is provided with a regulated DC input voltage, and power conditioning equipment within the power subsystem and at each load is included. Post regulators within the loads are not considered for weight or reliability, since they would be required for any distribution system. However, their inefficiency is considered to establish the quantity of power required from the source.

Post regulators within each load are considered to establish total power requirements, but are not considered for weight or reliability since they are common to either distribution system.

The AC distribution system consists of a main inverter in the power subsystem and a transformer, rectifier, and filter at each load. The two DC distribution systems shown were reviewed. The first consists of a DC to DC converter at each load, and the second consists of a single DC to DC converter in the power subsystem that provides all output voltage requirements. Power switching requirements are shown schematically as relay contacts.

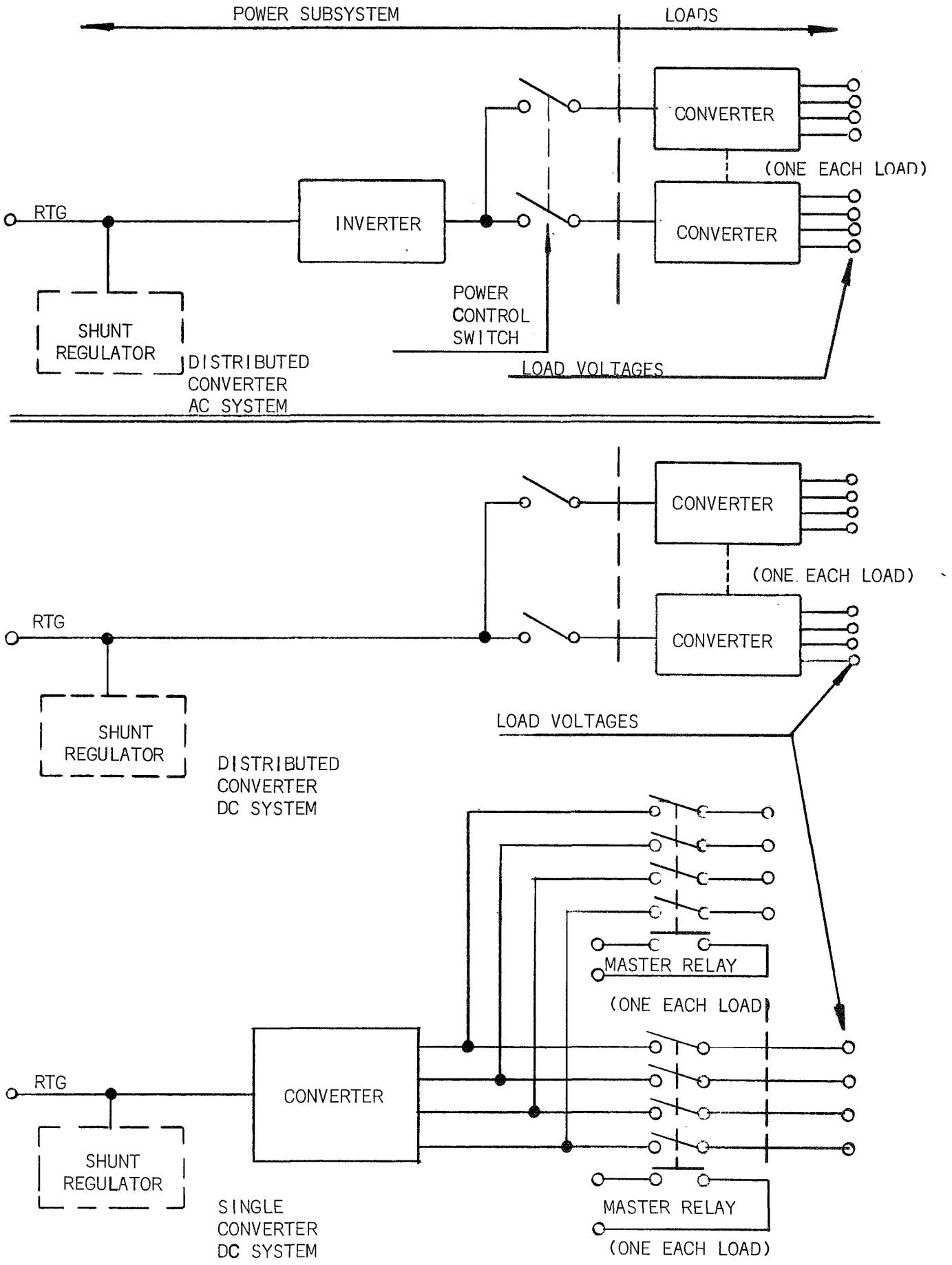


Figure 7-16. Alternative Power Distribution Systems

The functions required to process power to the desired load voltages are shown in Figure 7-17. A functional comparison is made between AC and DC systems. General weight trends and efficiencies are also shown for the DC case and are applicable for the equivalent function of the AC case. Note that all functions are sensitive to frequency such that either weight or efficiency is affected by a change in operating frequency. Note also that inefficiencies may be converted to additional source weight at a penalty of 1.2 watts per pound. Transformer weight and filter weight decrease as frequency increases. Switch efficiency decreases as frequency increases, and this results in increased power source weight. Therefore, as frequency increases, power system weight decreases due to lighter magnetic components, but increases due to switch inefficiencies. The summation of these effects results in an inversion frequency range where weight is considered minimized. This study is based on component designs that operate within this frequency range of minimum total system weight.

The differences between the two systems of Figure 7-17 are the additional power transformer required for the AC system which reduces overall efficiency and increases source weight, and the large number of DC to DC converter power oscillators (one per load) which, when packaged, increase overall weight. These power and weight differences were identified through load analysis and a review of power conditioning equipment to satisfy load requirements.

The distribution system was considered loss-less since it consists of relay contacts and wire. However, the weight of the centralized DC distribution systems exceeds the AC or DC distributed converter systems. Here a large number of relay contacts are required for each load (one for each voltage, and one master relay to interface with the command subsystem); and additional wiring is required to connect the multiple output voltages to user loads.

A parametric analysis of AC and DC distribution systems was performed to show system reliability as a function of inverter, transformer-rectifier, and DC to DC converter reliability. Using TOPS and Mariner failure rates, a relative reliability estimate of the functional components defined the region of interest within the parametric data. Redundancy was applied to selected loads. Growth effects were reviewed in order to identify the greatest system reliability improvements for increases in power conditioning equipment reliabilities. System operation under failure modes was identified. Consideration was given to system operation as a result of low source voltage during fault clearing, as well as fault clearing implementation.

Additional considerations are thermal control, voltage regulation, size, producibility and electromagnetic interference.

The frequency range where weight is minimized is from two to six kilohertz as discussed in Section 7.1. The inverter should operate near the high end of the minimum weight range, and at a multiple of 400 Hertz to minimize interaction with the attitude control system. Based on these considerations, 4800 Hertz is recommended. Of the three distribution systems reviewed, the centralized DC system

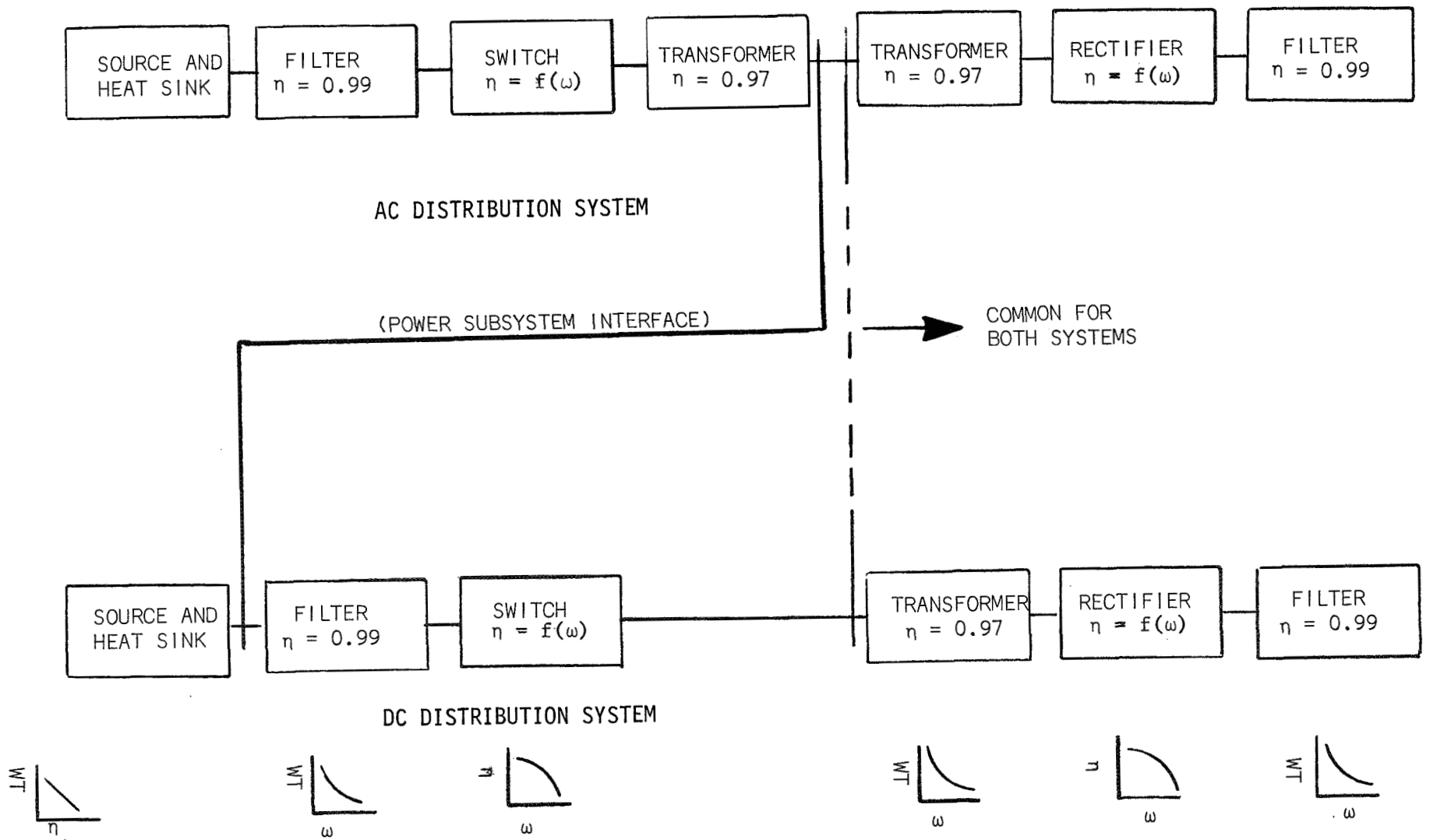


Figure 7-17. Functional Distribution Block Diagrams

was eliminated primarily because of the larger number of relays required for load control and its resulting lower reliability. A decentralized power processing configuration is essential for reliable fault clearing. The AC system should be divided into several small inverters to provide the same decentralization as the DC system. Since the DC system provides the greatest decentralization, and since it is favored in many of the system parameters studied, the recommendation is that a distributed converter DC distribution system be developed for TOPS.

System parameter comparisons are tabulated in Table 7-5. The distribution systems are distributed DC, AC and centralized DC. Thirty-two loads can be supplied directly with either AC or DC voltage. Redundant power conditioning may be required for eleven of these loads. Table 7-6 is a listing of loads where redundancy may be indicated.

The power shown is the source power required for each system. It is based on a load analysis of voltage, power and regulation at each voltage. For the AC and DC systems, load requirements were satisfied; however, for the centralized DC system voltages were selected based on common use and DC to DC converters were applied for voltages greater than 35 volts. Figure 7-18 is a functional block diagram of a DC to DC converter with a series post regulator showing the method of calculating power. Where regulation better than five percent was required, a minimum fixed loss of two volts was used for the series regulator. The efficiency of filters and transformers is fixed as a design requirement. The efficiency of diodes is determined by a fixed voltage drop of 0.8 volts. The efficiency of each power transistor switch was determined from the frequency analysis at five kilohertz. For low power DC to DC converters (less than 5 watts) the power transistor switch efficiency was modified as shown in Figure 7-19to account for fixed oscillator losses.

The power source requirement for the centralized DC system is the lowest. The distributed converter DC system power is higher due to the lower efficiencies of each low power DC to DC converter and the lower efficiencies assumed for science power conditioning. The AC system source power is greater than either DC system due to the addition of a power transformer in the main inverter.

The DC system is more efficient and is preferred over the AC system because the power margin is greater for a fixed power source.

Weight

System weight considerations are shown in Table 7-7. Each distribution system is represented by a functional description which is comparable to the block diagrams of Figure 7-17. As was discussed in the analysis approach, only those items which contribute to weight differences are compared. The differences occur in

- Source due to differences in efficiencies of the distribution systems
- Power Transistors, due to the larger number in the distributed DC system, compared with the one set in the distributed AC or centralized DC system
- Power Transformer, due to the extra main power transformer in the distributed AC system

Table 7-5. System Comparison

DISTRIBUTION SYSTEM / FACTOR	DISTRIBUTED DC		DISTRIBUTED AC		CENTRALIZED DC	
	SIMPLE	REDUNDANT	SIMPLE	REDUNDANT	SIMPLE	REDUNDANT
LOADS	32 LOADS - 11 REDUNDANT (43 TOTAL)					
RTG POWER (WATTS)	252		258		246	
WEIGHT (POUNDS)		13.9		18.1		21.5
SIZE	G E N E R A L L Y E Q U A L					
RELIABILITY ELECTRONIC PARTS COUNT	1920	2580	1544	2122	2318	3240
RELAYS	43		43		147	
SYSTEM	.74		.75		-	
POWER SYSTEM	HIGH		-		-	
OPERATION	FAILURE EFFECTS - POWER LOSS & FAULT PROTECTION					
THERMAL CONTROL	HEAT LOSS DISTRI-BUTED 10-15%		HEAT LOSS 8-10% P.S. 5-7% DISTRIBUTED		HEAT LOSS LOCALIZED 10-15%	
REGULATION (PERCENT)	.7 - .9		2.4 - 2.5		3.0 - 4.5	
EMC	RADIATION				MUTUAL COUPLING (CONDUCTIVE)	
PRODUCIBILITY	32 DC DC CONVERTERS 5 INVERTER TYPES		32 TRANSFORMER-RECTIFIER 1 INVERTER TYPE		1 TYPE	
SWITCHING	CIRCUIT DEVELOPMENT		CIRCUIT DEVELOPMENT			

Table 7-6. Loads with Redundancy Requirements

TELEVISION A
TELEVISION B
SCIENCE DATA SUBSYSTEM
FLIGHT TELEMETRY SUBSYSTEM
DATA STORAGE SYSTEM
CENTRAL COMPUTER & SEQUENCER
COMMAND SUBSYSTEM
CANOPUS SENSOR
AC ELECTRONICS
AC GAS VALVES
PYRO CONTROL

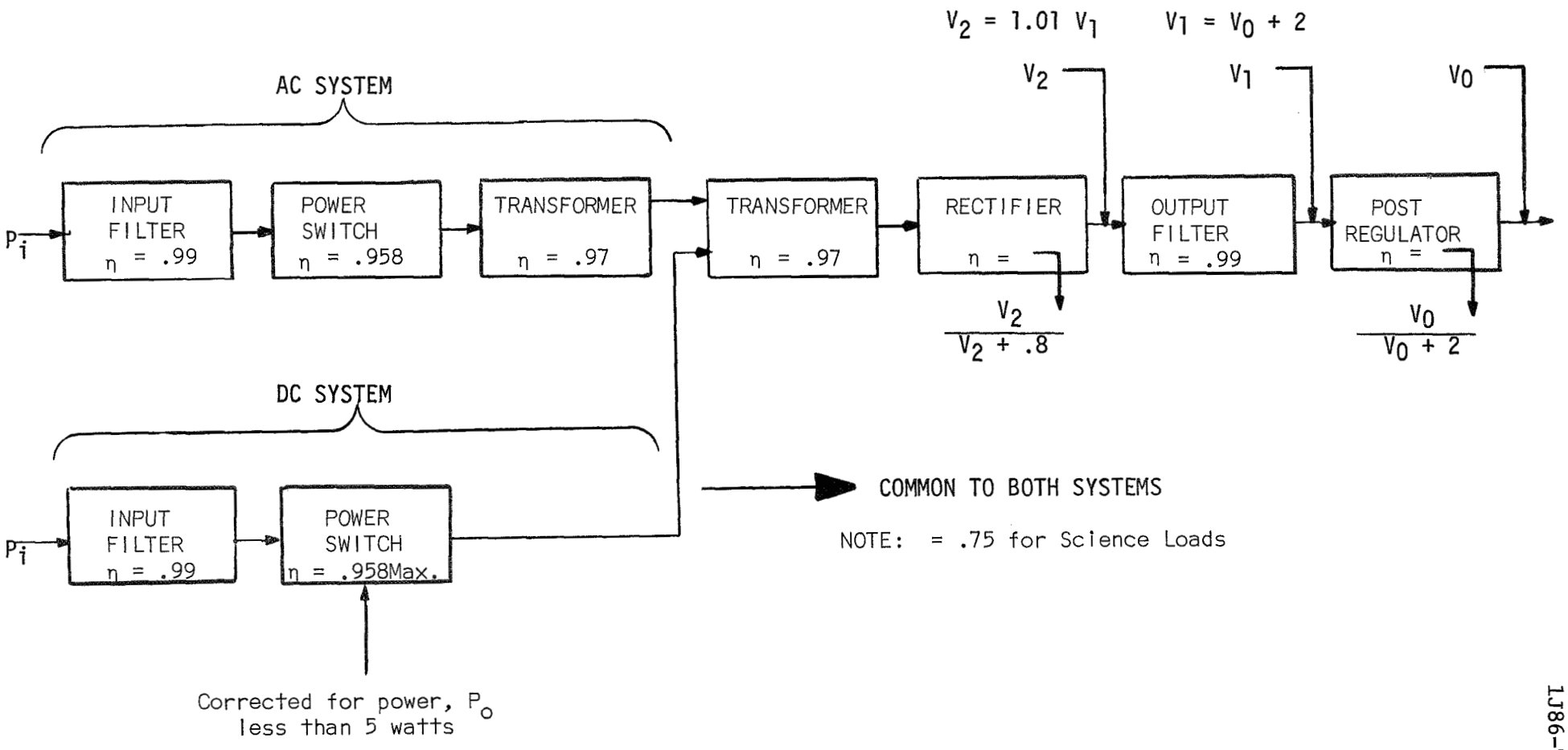


Figure 7-18. Power Calculation Block Diagram

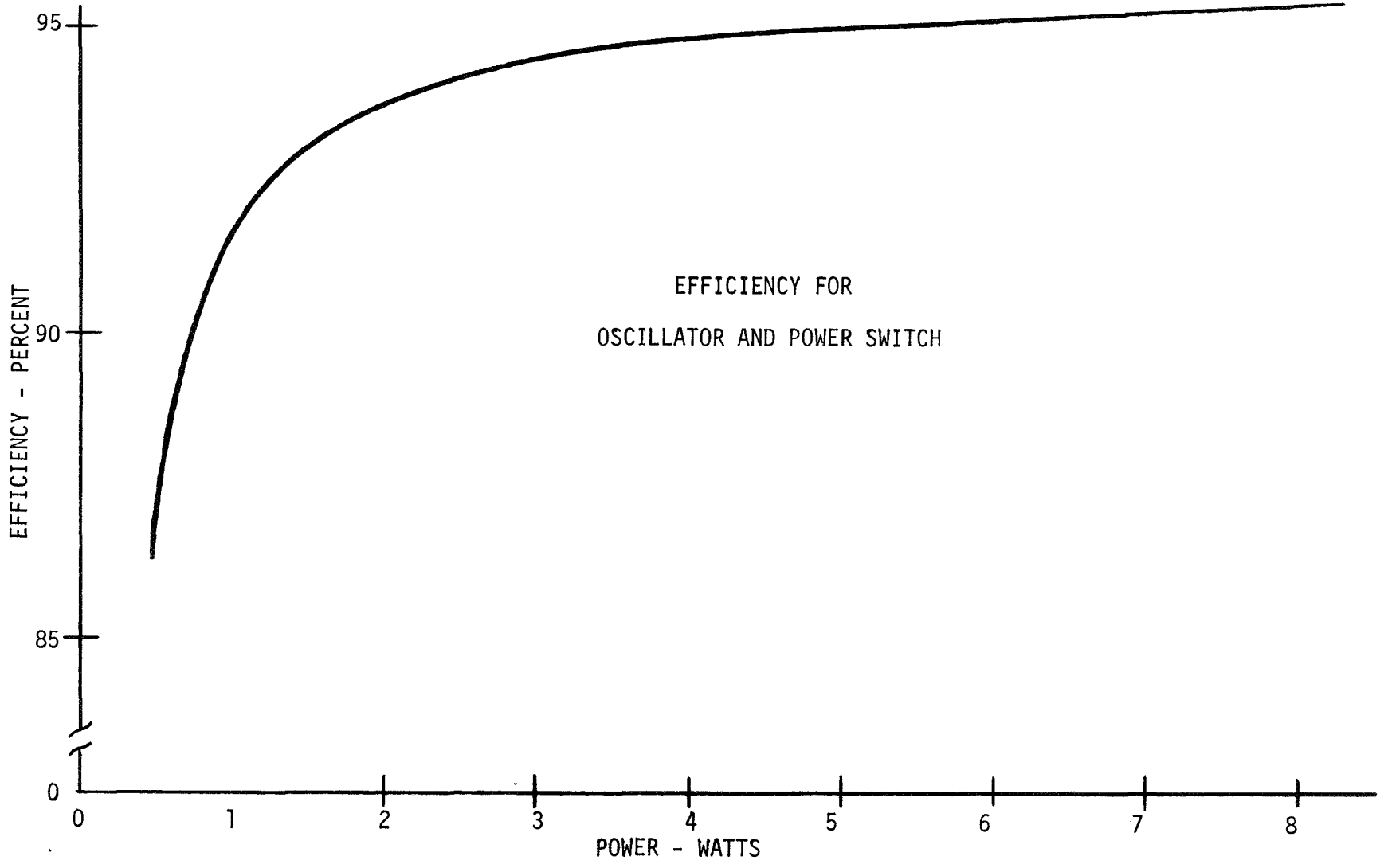


Figure 7-19. Power Transistor Efficiency

Table 7-7. Weight Considerations

DISTRIBUTED DC	DISTRIBUTED AC	CENTRALIZED DC
SOURCE (252 Watts)	SOURCE (258 Watts)	SOURCE (246 Watts)
DISTRIBUTION RELAY HARNESS	DISTRIBUTION RELAY HARNESS	DISTRIBUTION RELAY HARNESS
INPUT FILTER	INPUT FILTER	INPUT FILTER
TRANSISTOR OSCILLATOR	TRANSISTOR OSCILLATOR	TRANSISTOR OSCILLATOR
--	TRANSFORMER	TRANSFORMER
TRANSFORMER	TRANSFORMER	--
RECTIFIER	RECTIFIER	RECTIFIER
OUTPUT FILTER	OUTPUT FILTER	OUTPUT FILTER
POST REGULATOR	POST REGULATOR	POST REGULATOR
HEAT SINK	HEAT SINK	HEAT SINK

 SHOWS COMMON ITEMS NOT USED FOR WEIGHT COMPARISON

DIFFERENCES ARE:

- SOURCE POWER REQUIREMENTS
- TRANSISTORS, OSCILLATORS, AND TRANSFORMERS
- DISTRIBUTION RELAYS AND WIRING
- HEAT SINK REQUIREMENTS

- Power distribution, due to the harness and relay switching for the centralized DC system. The distributed DC and AC systems are assumed to have equal weight distribution equipment.

- Heat sink, due to the weight penalty associated with dissipating the extra watts lost.

The common items not included are:

- Source, due to the total source weight

- Filters, since filter requirements are assumed equal for all systems

- Low power transformers, since the remote transformers in the distributed AC system and the converter transformers in the distributed DC system are assumed equal.

- Rectifier weights, since these are negligible relative to the power transistor switches.

- Switching frequency, since system weight is considered constant within a given frequency band (see Section 7-1).

For discussion purposes the distributed DC system is the reference system. With a design source penalty of 1.2 watts per pound (0.83 pounds per watt) and a heat sink penalty of 0.07 pounds per watt, the distributed AC system requires six additional watts at a total penalty of 0.9 pounds per watt, or 5.4 pounds more weight than the distributed DC system. Similarly, the centralized DC system is more efficient and requires six less watts or 5.4 pounds less than the distributed DC system. The detail weight breakdown is summarized in Table 7-8. On a system basis, the distributed DC system results in a lower weight. The primary difference is the source penalty of 5.4 pounds applied to the distributed AC system for its lower efficiency. The additional distribution penalty required for the centralized DC system makes it less attractive than either distributed system.

The size effects are discussed by a comparison of the additional large size piece parts, such as relays, filters, and transformers. The additional volume required for the many oscillators of the DC system may be considered a small addition to the transformer-rectifier assembly of the distributed AC system. The centralized DC system is considered to have the smallest power conditioning equipment requirements, since packaging efficiency of a single large unit is greatly improved over multiple units for either the distributed AC or DC systems. However, the size required for additional relays and related distribution and controls is greater; therefore, the size is considered equal to the distributed AC or DC systems.

The distributed DC system has the potential for providing the lightest weight system, and is the preferred system from a weight standpoint.

Table 7-8. Weight Summary

	DISTRIBUTED DC		DISTRIBUTED AC		CENTRALIZED AC	
CONFIGURATION	SIMPLE	REDUNDANT	SIMPLE	REDUNDANT	SIMPLE	REDUNDANT
POWER CONDITIONING	8.02	8.02	6.80	6.80	8.40	8.40
RELAY(1)	2.20	4.40	2.20	4.40	7.35	14.70
HARNESS(2)	1.08	1.08	1.08	1.08	2.80	2.80
CONNECTOR	.40	.40	.40	.40	1.0	1.0
SOURCE AND HEAT SINK PENALTY	--	--	5.40	5.40	-5.40	-5.40
TOTAL WEIGHT (POUNDS)	11.70	13.90	15.88	18.08	14.15	21.50

(1) *RELAY - .05 Pounds Per Relay and Relay Driver*

(2) *HARNESS - 5 Foot Average Length to Loads*

Twisted Pair for the Distributed DC and AC Systems

Multiple Twisted Triplet for the Centralized DC System

Reliability

Indicators of system reliability are gross parts count, applied redundancy, application of failure rates to reliability calculations, sensitivity to changes in component reliability, and system operation. These factors have all been considered and are now discussed.

Parts Count

Typical circuits were reviewed for application to the functional blocks shown in Figure 7-17. Figure 7-20 is a parts count breakdown for each circuit function. Figure 7-21 shows relay and relay driver circuits piece part requirements for redundant and non-redundant switched loads.

The total parts count includes the power conditioning equipment and the relay circuits. Both the distributed AC and DC systems require the same number of relays since each requires only one pair of lines per load. The centralized DC system requires more relays since multiple lines are transferred to each load, and a master relay is required to interface with a single command. Since the centralized DC system has the greatest number of relays, its piece part count is high even though the power conditioning equipment has relatively few parts. The distributed AC system has the fewest piece parts because a main inverter is used, while for the distributed DC system an individual converter at each load is required.

Application of the piece part failure rates shown in Table 7-9 was performed to determine the relative reliability of each component. This table combines the TOPS failure rates from Table 7-1 of the first Quarterly Technical Report with some additional piece part information, and compares this with TRW data used in the Mariner Mars power system study. For system comparison the reliability models used are shown in Figure 7-22. Perfect failure detecting and switching is assumed for redundant configurations since these should be an order of magnitude more reliable than the functional component protected in order to effectively improve reliability in a redundant configuration. Parametric data was generated showing system reliability (Rs) for various inverter reliabilities (Ri) as a function of transformer rectifier reliability (Rt) and DC to DC converter reliability (Rc). The parametric data was generated using parallel redundancy rather than standby redundancy because the reliability difference is small for low values of λ t. (refer to Figure 7-23, and the derivation of Figure 7-24).

Applying the calculated component reliability to the system parametric curves provides the system reliability for distributed AC or DC systems. The centralized DC system was not evaluated further because the electronic piece part count is greatest and the larger sub set of the total is the relay, the piece part with the highest failure rate. The centralized DC system automatically becomes the least reliable system when relay failure rates are considered. Further consideration of the centralized DC distribution system was not necessary since both distributed AC and DC systems require one relay and one pair of wires per load. Therefore, the data in Figure 7-25 and 7-26 consists of parallel redundancy with perfect switching only for the distributed AC and DC systems.

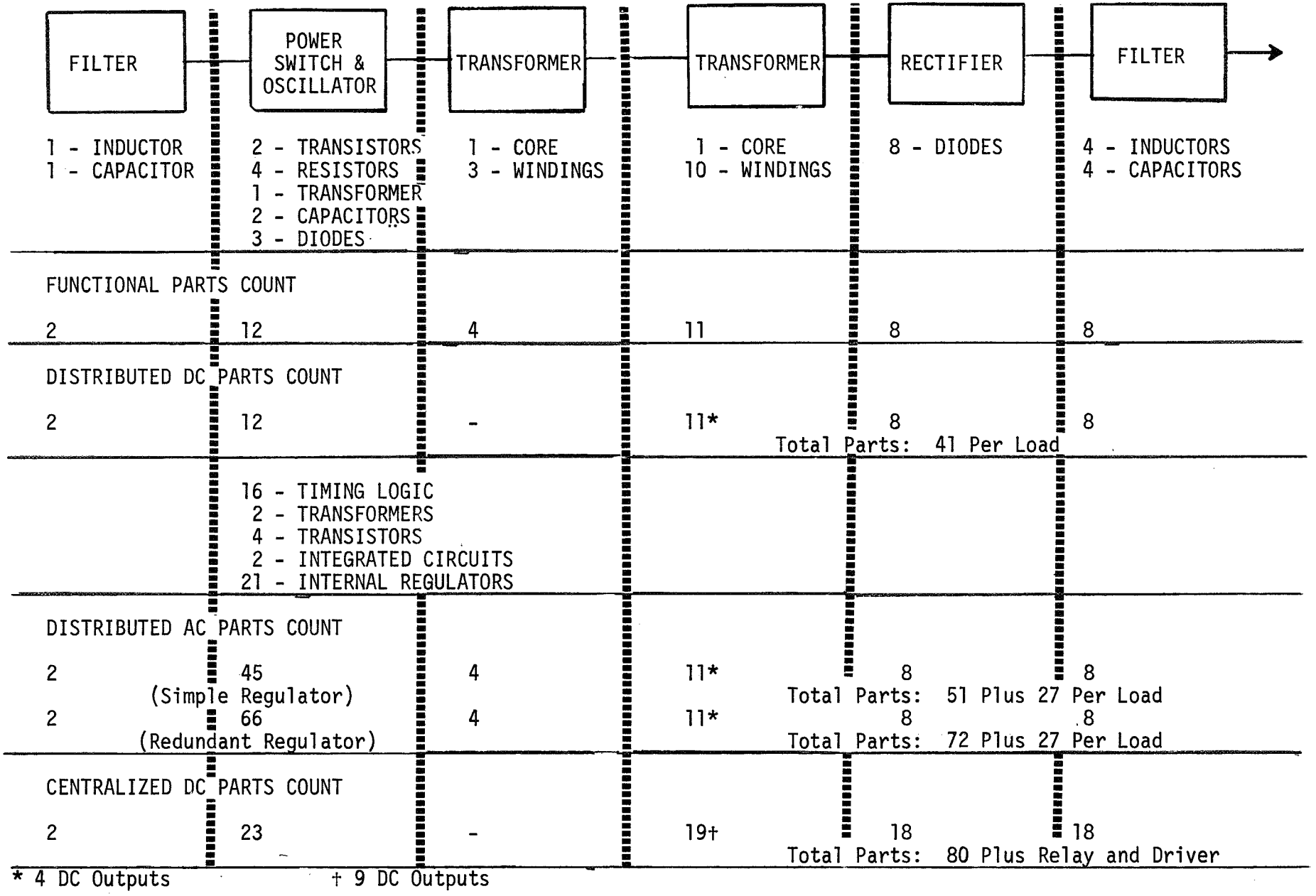


Figure 7-20. Relative Distribution System Parts Count

DRIVER PARTS COUNT

2 TRANSISTORS

6 RESISTORS

4 DIODES

4 CAPACITORS

2 INTEGRATED CIRCUITS

1 RELAY

19 PARTS PER RELAY

RELAY CONTACT CONFIGURATION

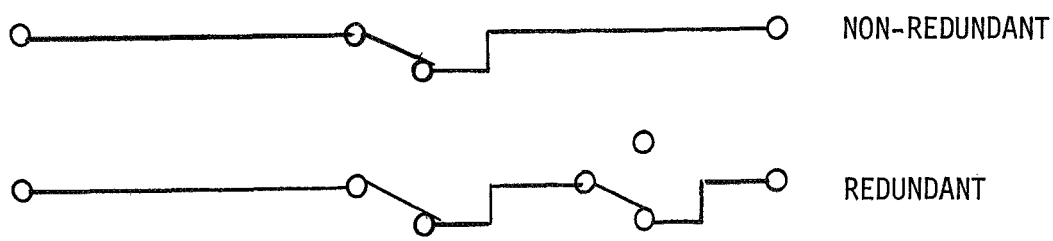


Figure 7-21. Relay Circuit Piece Part Requirements

Table 7-9. Part Failure Rate Data for the Distribution Study

Part Type	Failure Rate x 10^{-6} Failures per Hour	
	TOPS	TRW
Capacitors		
Glass	.002	.002
Ceramic	.005	.015
Foil	.008	.040
Tantalum		
Solid	.01	.021
Wet	.1	.014
Diodes		
Signal & Switching	.01	.013
Zener	.02	.060
Power	.05	.014
Resistor		
Carbon Composition	.001	.0070
Film	.008	.0014
Wire Wound	.09	.0650
Transistors		
Small Signal bi-polar	.02	.010
Power Bi-polar	.08	.056
JFET	.02	
Isolated Gate FET	.05	
Si Controlled Rectifier/Switch	.07	
I/C's (does not include MSI/LSI)		
Bi-polar Monolithic	.2	.05
MOS Monolithic	.4	.05
Relays (Mech)	2.0	.20
Transformers		
Power >1.0 Watt Dissipation	.08	.015
Power <1.0 Watt Dissipation	.02	.015
Inductors		.015

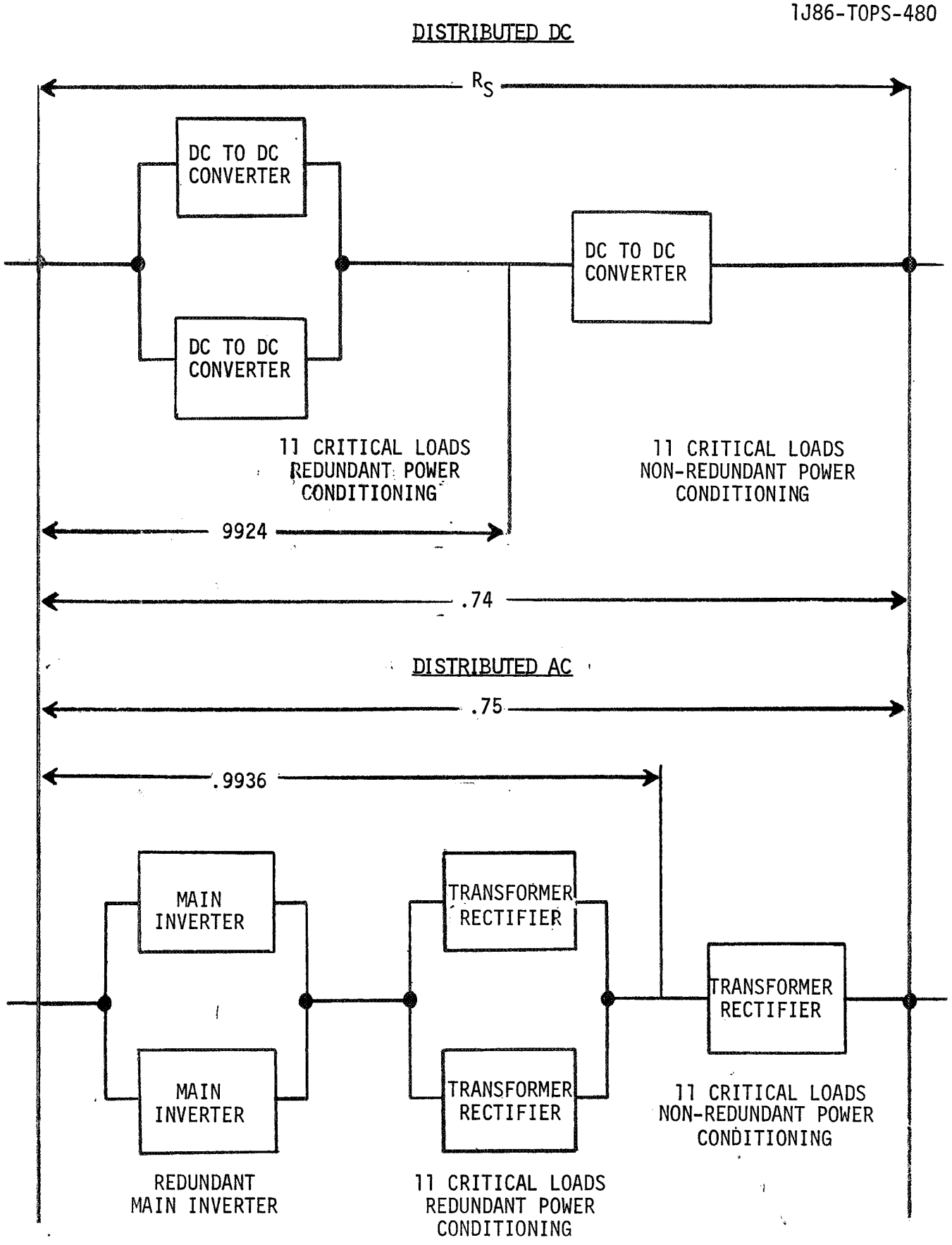


Figure 7-22. System Reliability Models

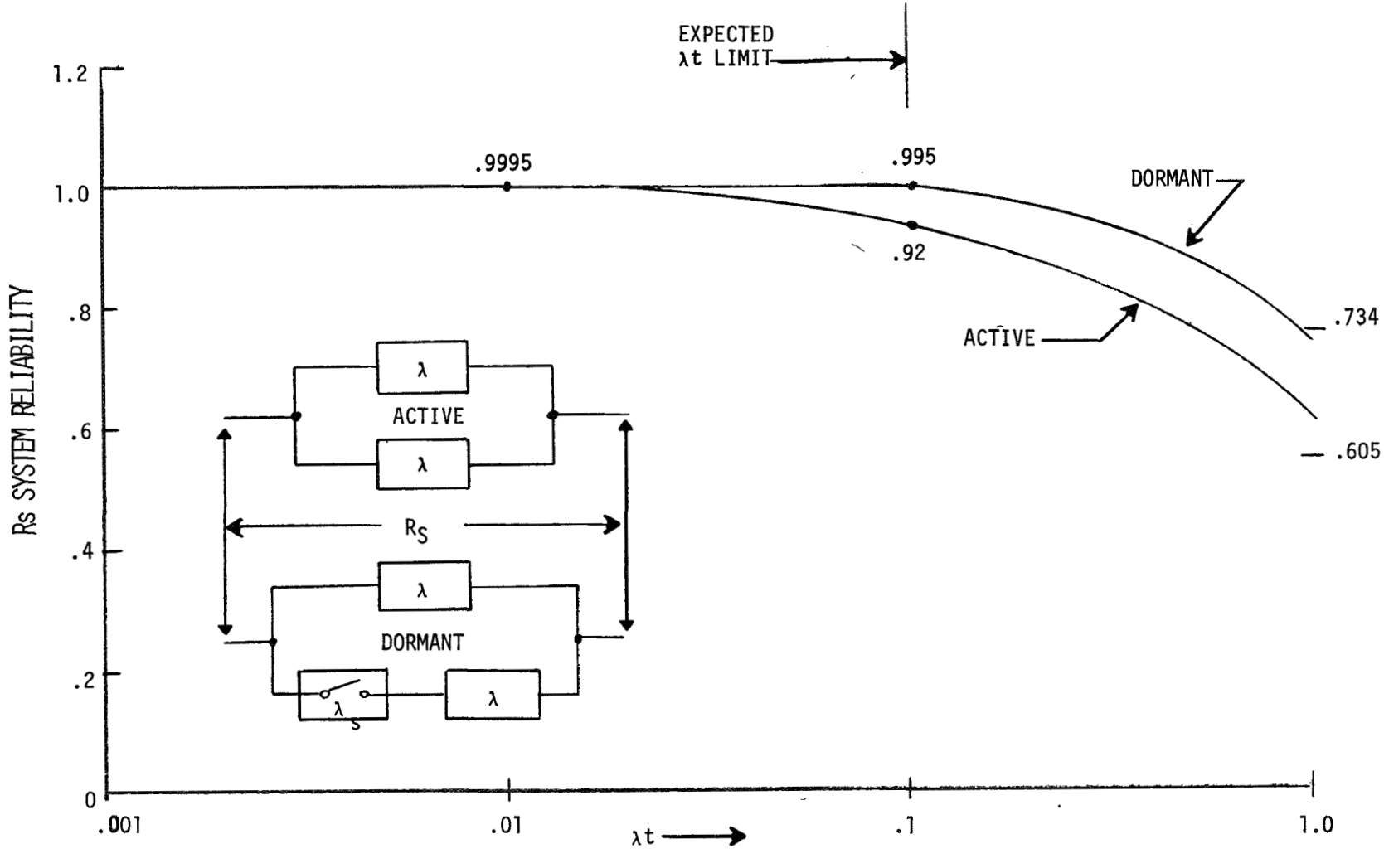


Figure 7-23. Redundancy Comparison

FOR ACTIVE REDUNDANCY (R_A):

(7-43) $$R_A = 2e^{-\lambda t} - e^{-2\lambda t}$$

FOR DORMANT REDUNDANCY (R_D):

(7-44) $$R_D = e^{-\lambda t} + \lambda t e^{-(\lambda+\lambda_s)t}$$

WHERE: λ = FAILURE RATE OF UNIT

λ_s = FAILURE RATE OF SWITCH

t = MISSION TIME

FOR $R_D > R_A$:

(7-45) $$e^{-\lambda t} + \lambda t e^{-(\lambda+\lambda_s)t} > 2e^{-\lambda t} - e^{-2\lambda t}$$

AND THIS REDUCES TO:

(7-46) $$1 + \lambda t e^{-\lambda_s t} > 2 - e^{-\lambda t}$$

AND THIS REDUCES TO:

(7-46) $$1 + \lambda t e^{-\lambda_s t} > 2 - e^{-\lambda t}$$

FOR $\lambda_s = 0$, (PERFECT SWITCHING)

(7-47) $$1 + \lambda t > 2 - [1 - \lambda t + (\lambda t)^2/2! - (\lambda t)^3/3! \ldots.]$$

(7-48) $$1 + \lambda t > 1 + \lambda t - (\lambda t)^2/2! + (\lambda t)^3/3! \ldots.$$

AND THIS IS TRUE FOR ALL VALUES OF λt.

HOWEVER, IF λt IS SMALL:

(7-49) $$1 + \lambda t \approx 1 + \lambda t - (\lambda t)^2/2! + (\lambda t)^3/3! \ldots.$$

AND $$R_D \approx R_A$$

Figure 7-24. Derivation of Redundancy Reliabilities

The system reliability of Figure 7-25 is based on 11 critical redundant loads and 11 science non-redundant loads supplied from either a redundant main inverter in the distributed AC system or DC to DC converters in the distributed DC system. The curve Ri = 1.0 is the distributed DC system; the other curves are for various inverter reliabilities. For this system definition the distributed AC system is slightly more reliable. When only the critical loads are considered as shown in Figure 7-26, the system reliability is greater and the distributed AC system is again slightly more reliable. Although the parts count suggests a large reliability difference, the calculated difference is relatively small.

Reviewing reliability from a growth aspect is accomplished through sensitivity studies. Figure 7-27 is a set of parametric curves similar to those previously discussed. Given an arbitrary system reliability, Rs = .988, and using the estimated inverter, transformer-rectifier, and DC to DC converter reliabilities, improvement in component reliability is necessary for either the distributed DC or AC system in order to satisfy the assigned system reliability, Rs. The system requiring minimum component improvement is an indication of the potentially more reliable system.

Point (1) represents the distributed DC system, and the DC to DC converter reliability increase (ratio of unreliability) required is from 0.968 to 0.975 (a ratio of 1.3). Point (2) represents the distributed AC system reliability for an inverter of 0.9 reliability. For a constant transformer-rectifier reliability the inverter reliability would have to increase to Point (2'), i.e., from 0.9 to 0.94 (a ratio of 1.7). For a constant inverter reliability the transformer-rectifier reliability would have to increase by an order of magnitude (a ratio of 23). Note that any improvement in transformer-rectifier reliability is also an improvement in DC to DC converter reliability. Therefore, for the distributed AC system to result in a higher reliability growth than the distributed DC system the reliability growth has to be in the inverter. Since the distributed DC system increase is less than the distributed AC system, the distributed DC system has the potential for providing the highest system reliability.

This aspect may be visualized easily when considering derating factors for many DC to DC converters compared with a single main inverter. For example, the use of a five ampere transistor at less than one ampere greatly improves reliability of the power oscillator of the DC to DC converter. Contrast this with the minimum derating for the main inverter due to the availability of parts. A thirty ampere transistor operating at eight amperes results in less relative derating making the distributed AC system more difficult to improve. Further reliability growth could be realized in the distributed DC system through integrated circuit techniques for the power oscillator of each DC to DC converter. This would reduce the difference between the transformer-rectifier and the DC to DC converter reliability. This type of improvement is impossible to attain in the distributed AC system because of the high power level of the main inverter.

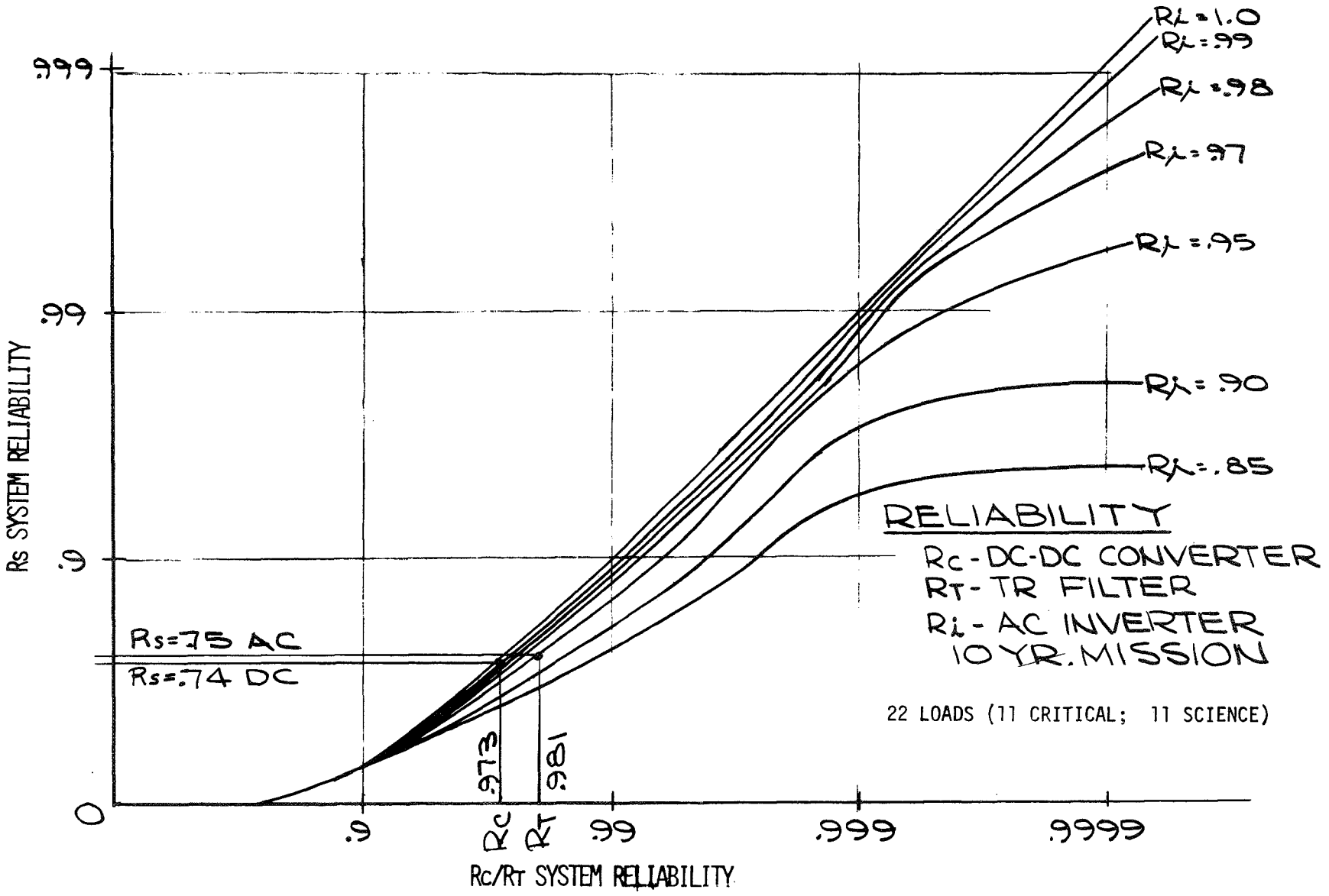


Figure 7-25. System Reliability Considering All Loads

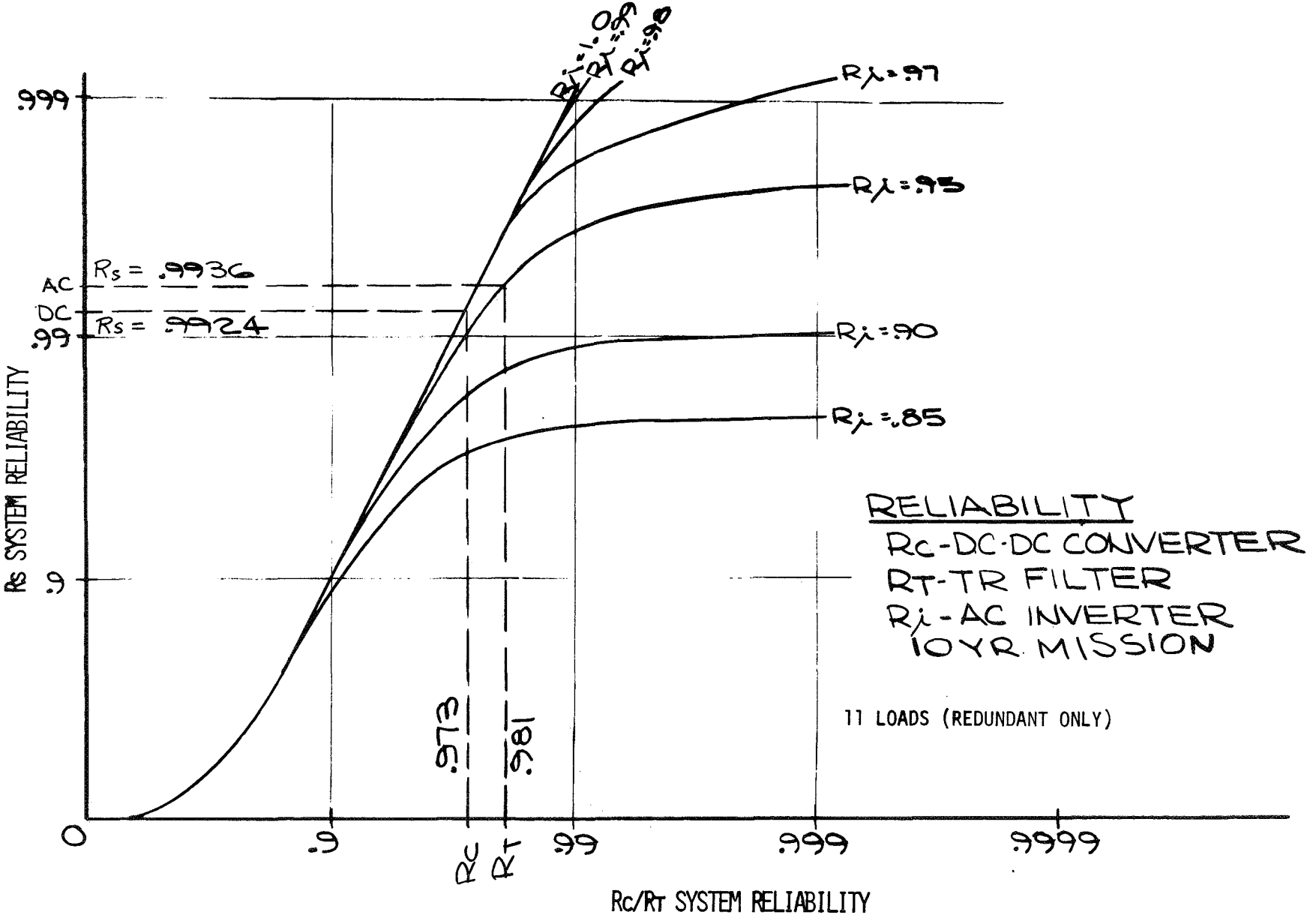


Figure 7-26. System Reliability Considering Critical Loads

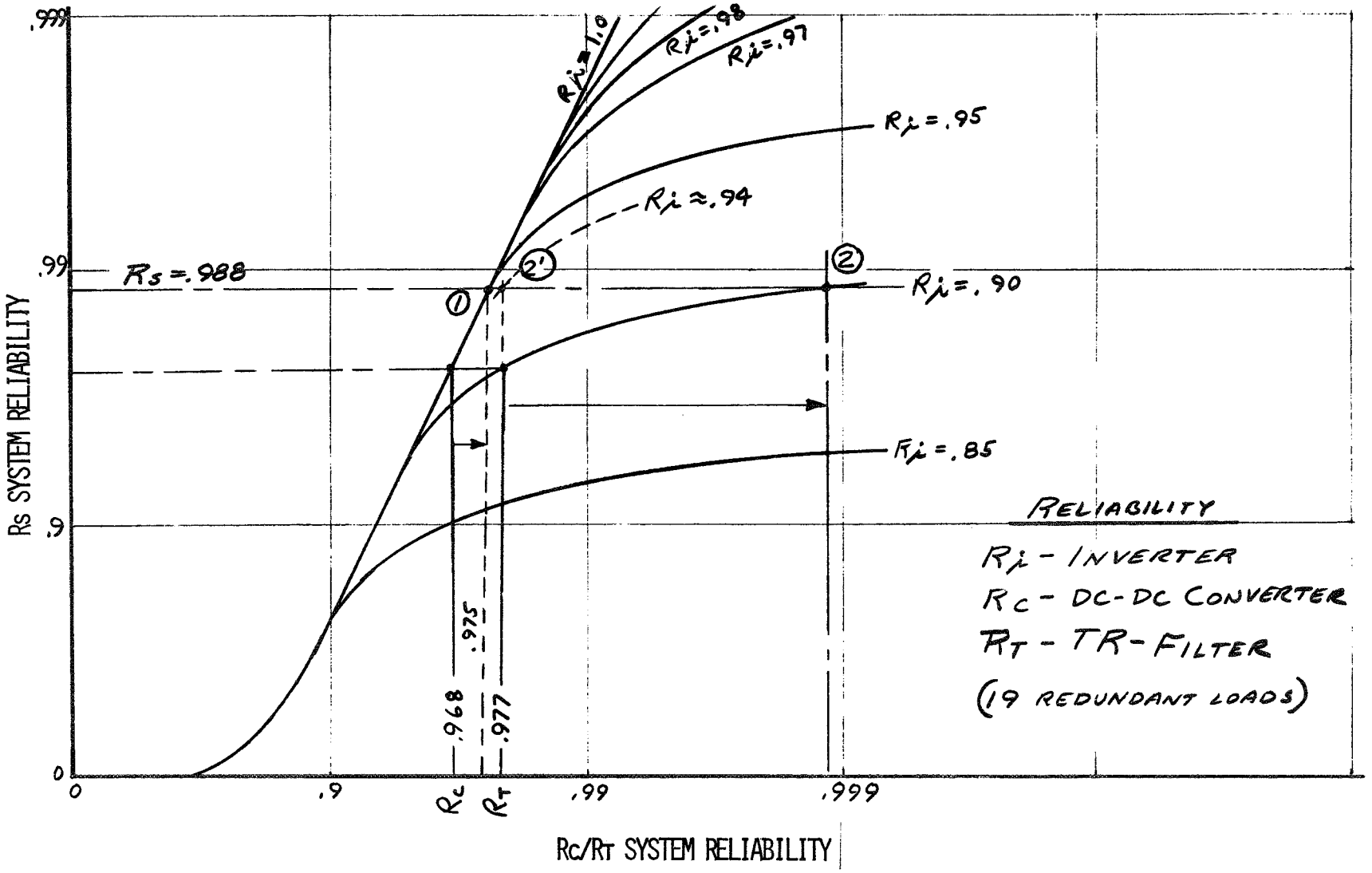


Figure 7-27. System Reliability Improvement and Growth

In summary, the centralized DC system was considered less reliable than the distributed DC or AC system; therefore, further analysis was terminated. The piece part count of the distributed AC system is less than the distributed DC system, but the calculated reliability without applying derating factors shows little difference between the two approaches. Consideration of reliability growth does, however, show that a greater system reliability is potentially available for the distributed DC system. The next aspect of reliability to be considered is the operational system - particularly during failure modes.

System Operation

A failure modes and effects reliability analysis provides system or component considerations that reduce the effects of some failure modes. Serious failure modes for TOPS power subsystem are those that result in load changes causing the source voltage to exceed the regulated voltage tolerances. Both load reduction and load increase will affect the delivered power, but the shunt regulator will limit the voltage excursion for load reduction. Therefore, only increasing load faults are considered in this analysis.

Typical source BOM and EOM characteristics are shown in Figure 7-28. These characteristics are modified by the shunt regulator to maintain constant voltage within source capability. Two load lines are shown, total load and the inverter load only. The inverter load makes up much of the total load.

The system operational requirements are that load faults shall not result in power subsystem degradation and that normal operation resume after fault removal. A second requirement is that a power conditioning failure shall be detected and the faulty unit removed from the bus. Probable failure of loads and of the power conditioner are that the reflected load impedance could approach zero. Under this failure the source voltage could decrease to zero making failure detecting and fault removal without energy storage impossible. Therefore, fault detection and protection for power conditioning may be either a fuse or a circuit breaker.

For the purpose of this example in the distributed AC system, the fuse rating would be twice the normal load (eighteen amperes) if the load fault protective device were a fuse. Two fault lines are shown crossing the BOM and EOM characteristic at the eighteen ampere limit. Load faults in excess of these result in inverter input current greater than the inverter protective device rating. Under these conditions the inverter fault protective device rating will be exceeded and degradation may occur. If the inverter fault protection device were a circuit breaker, faults greater than those shown will result in race conditions between load fault protective device and inverter protective device. Regardless of protective device the inverter input current should not exceed the protective device rating for load faults. To satisfy this requirement an overload characteristic could be incorporated as part of the inverter. This characteristic is shown in Figure 7-29.

The inverter fault protective device may be either a fuse or a circuit breaker. The source short circuit current is 24 amperes. With a faulted inverter the current ratio of fault clearing to fault rating is 1.3. This ratio is not adequate for fuses and marginal for circuit breakers, particularly in the light of probable inverter load growth. In order to provide inverter fault removal and inverter

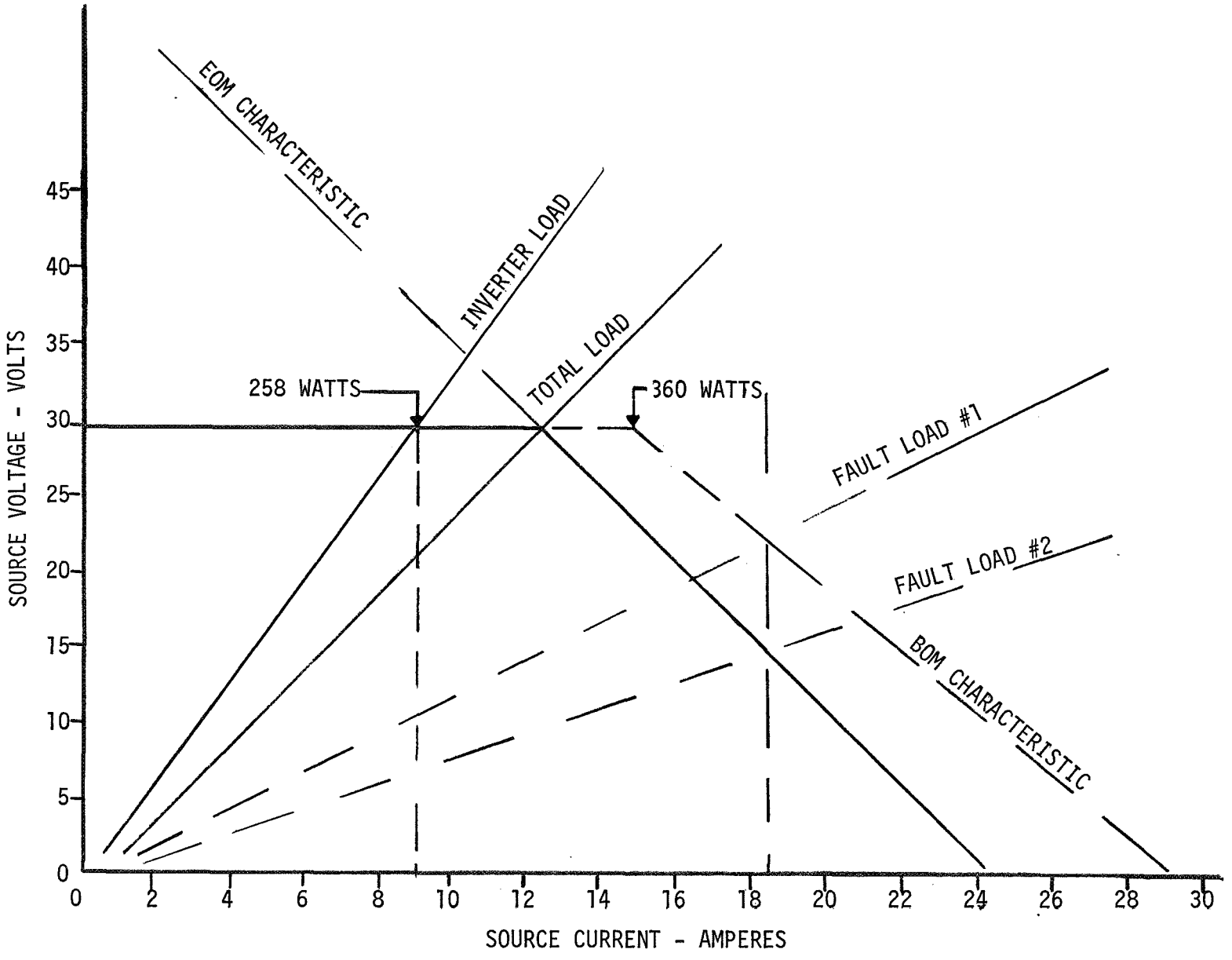


Figure 7-28. Source Operating Characteristic

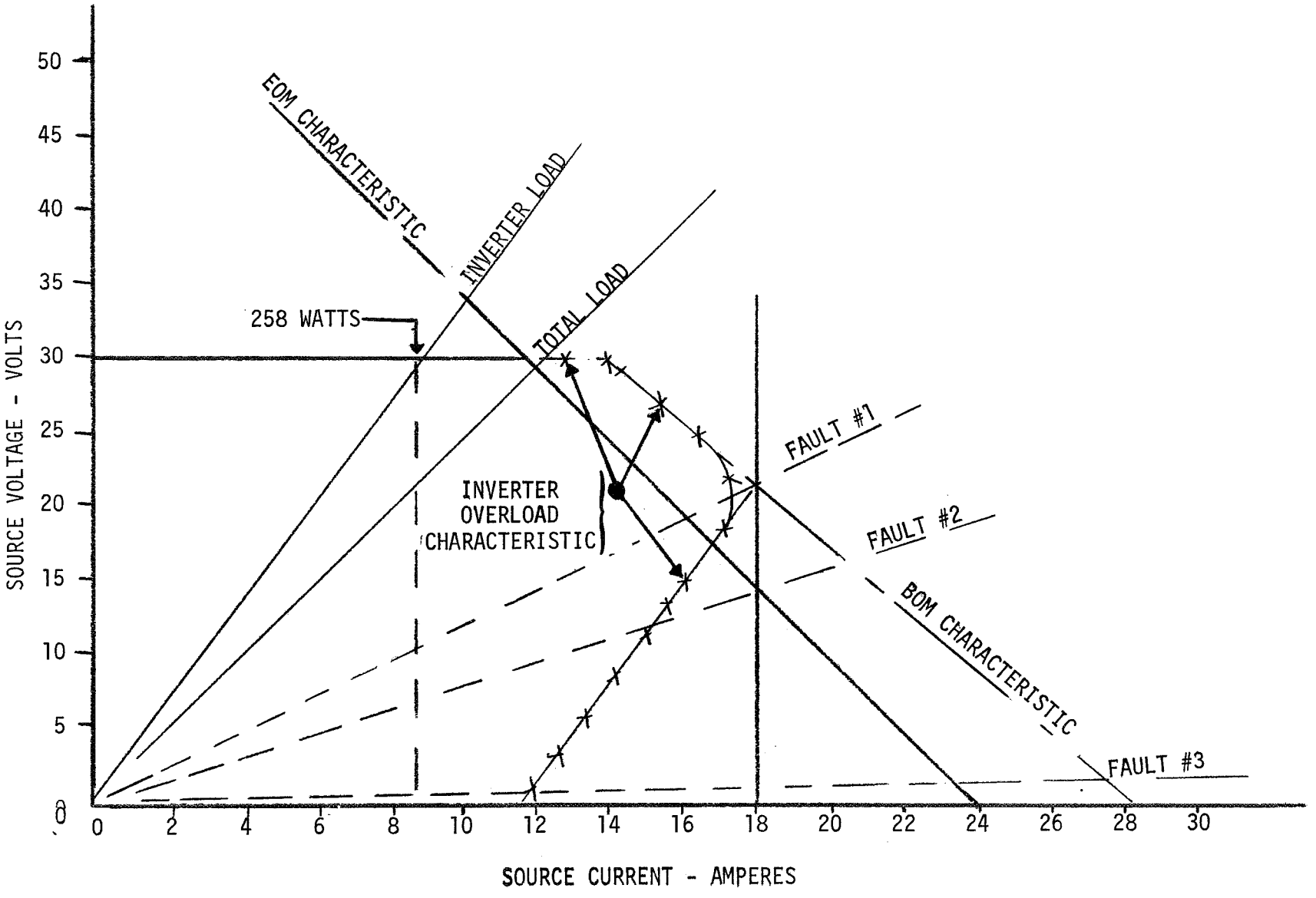


Figure 7-29. Source-Inverter Operating Characteristic

load growth, the inverter function should be divided into more than one unit. The smaller inverters and its load then represent a smaller percent of the total load and may be protected at current levels well below the source capability which could assure fault removal. The distributed AC system reliability is reduced by this aspect. Figure 7-30 is a comparison of distributed AC systems containing one and four inverters.

A system containing a single inverter that experiences an inverter failure results in total power loss for all loads. Division of the inverter function reduces the effect of an inverter failure. Therefore, the recommendation is that the distributed AC system be distributed at both source and load ends. Since the distributed DC system provides the greatest decentralization, the distributed DC system is preferred from the standpoint of systems operation during failure modes.

Thermal Control

Spacecraft thermal design requires that all power dissipated within the spacecraft be controlled to maintain the vehicle and sensitive loads within prescribed temperature limits. Sensitive loads may require additional heater power. However, the majority of spacecraft loads require dissipation of normal power. Special design considerations are required for high power dissipating loads. If thermal loads are evenly distributed, special heat dissipating structures are reduced. The distribution system that tends to evenly distribute heat is preferred since the requirement for special thermal paths is minimized. Further, if the additional heater power for sensitive loads could be reduced by selection of a distribution system, the system that requires less power is preferred.

A system breakdown of spacecraft thermal input is shown in Figure 7-31. Approximately fifteen percent of the total power is lost through power processing in power conditioning equipment. The balance is dissipated within the load. A further breakdown of power processing power is shown for the distributed DC and AC systems and for the centralized DC system.

For the distributed DC system the total processing power is distributed according to load requirements. The power conditioning equipment located at the load will dissipate fifteen percent more power than a sensitive load which may be considered as a small additional burden for thermal control. However, for sensitive loads that normally require heater power, this dissipation may be viewed as additional thermal control power that will reduce the thermal control heater power requirements.

A main inverter efficiency of approximately ninety percent can cause a dissipation of up to 25 watts for the distributed AC system. This dissipation requires special thermal design considerations which would not exist if it were distributed among the user subsystems. The distributed DC system is preferred because the thermal burden is distributed more evenly without penalty, and the additional heat at the loads could reduce the thermal control power which might otherwise be required.

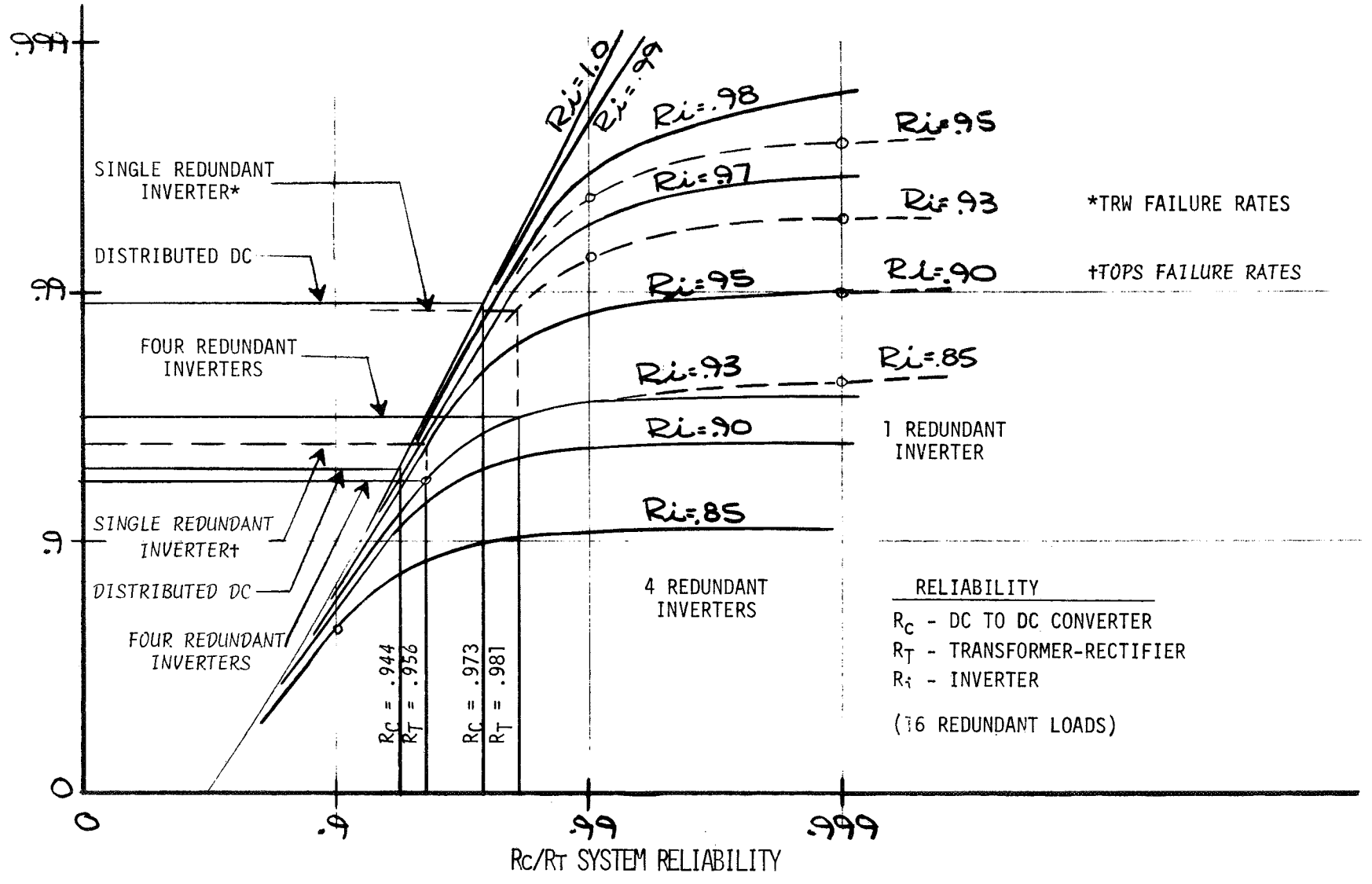


Figure 7-30. System Reliability with Multiple Inverters

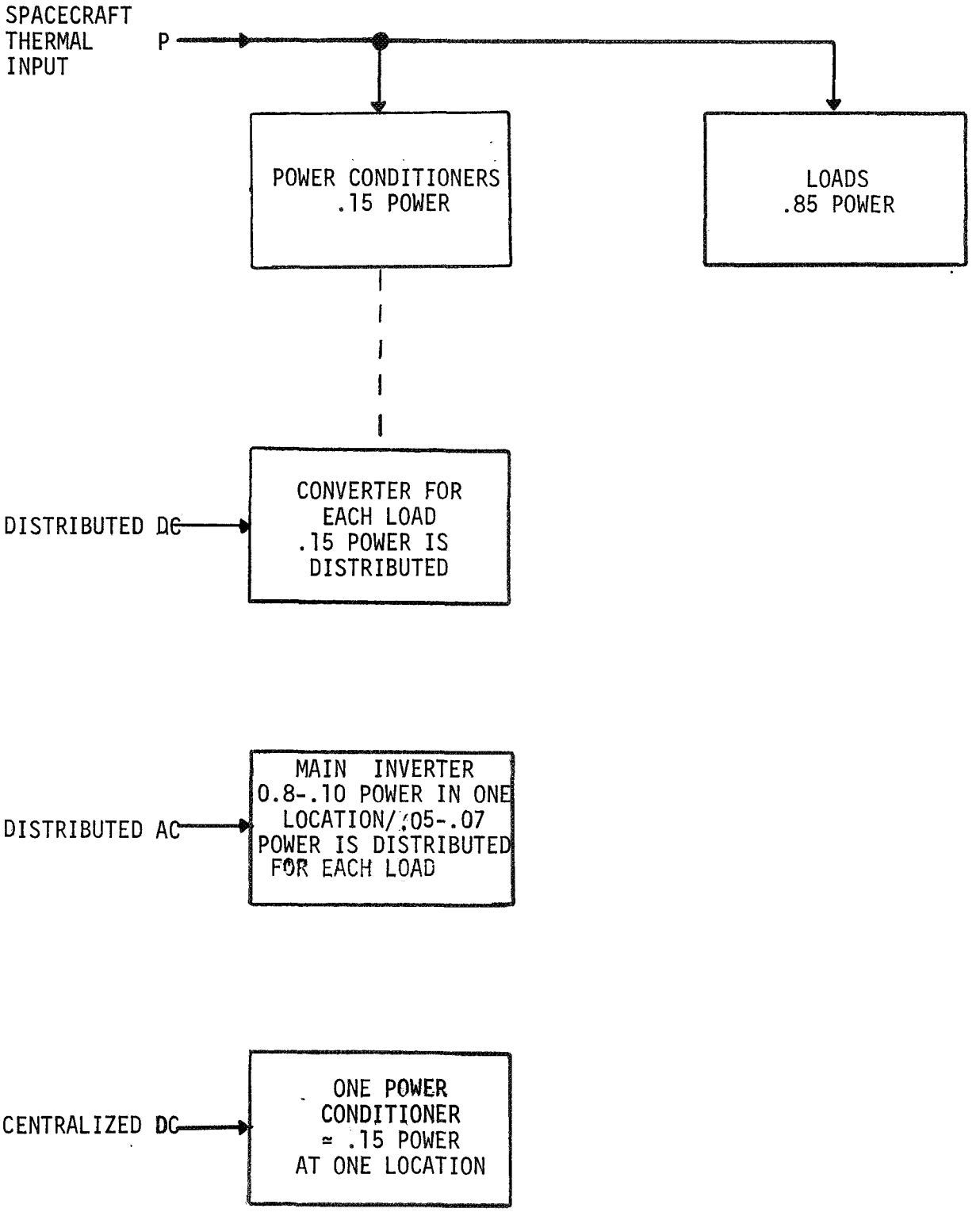


Figure 7-31. Thermal Control

Regulation

An assumption was made early in the study that post regulators would not be required for plus or minus five percent voltage regulation. Further, if tighter voltage regulation were required, post regulators would not be included in the analysis since these would be common to both the distributed DC and AC systems. A review of load regulation requirements shows that voltage precisions occur in the following steps: ten, five, two and one percent. A review of actual regulation capability for the distributed AC and DC systems was performed to identify the inherent regulation capability of these distribution systems.

The input voltage to both systems is maintained constant by the shunt regulator. Regulation at the load voltages, therefore, is determined by the load variations and the series resistance of the functional elements between the source and load. Both the distributed AC and the centralized DC systems experience wide load variations (approximately 2.5 to 1.0), while the distributed DC system has little load variation since each DC to DC converter is designed for a specific load requirement. For this reason, the distributed DC system regulation is better than either the distributed AC or the centralized DC system. The relative quality of regulation is shown in Table 7-10, Regulation Summary.

The distributed DC system provides typical regulation of less than one percent, indicating that post regulators will be necessary for very precise regulation only. For the distributed AC system, post regulators will also be necessary for two percent regulated outputs.

Since the distributed DC system provides a better quality of voltage regulation reducing the number of post regulators, the distributed DC system is preferred.

The regulation was derived from the series loss or voltage drop of the power conditioner functional elements. The efficiency is tabulated for reference, and the series loss is apportioned to the total loss of the functional element. For a load change of fifty percent the corresponding voltage change is also tabulated. Both the distributed AC and the centralized DC systems have been assigned a fifty percent load change, while the DC to DC converters of the distributed DC system have been assigned a ten percent load change.

The load change of ten percent is reflected through all of the functional elements. This load regulation is one fifth of the change experienced for a fifty percent load change for the other two distribution systems. These are tabulated and totaled for the distributed DC system.

The load change for the centralized DC system is also reflected through all of the functional elements. The fifty percent load change is reflected in the centralized DC column.

TABLE 7-10
REGULATION SUMMARY

FUNCTIONAL ELEMENT / PERCENT LOAD CHANGE	η	PERCENT SERIES LOSS	PERCENT LOSS CHANGE	DISTRIBUTED DC	DISTRIBUTED AC	CENTRALIZED DC
	-	-	50	10	50	50
INPUT FILTER	.99	1.0	0.50	0.10	0.50	0.50
POWER TRANSISTOR	.96	1.5	0.75	0.15	0.75	0.75
MAIN POWER TRANSFORMER	.97	1.5	0.75	-	0.75	0.75
REMOTE POWER TRANSFORMER	.97	1.5	0.75	0.15	0.15	-
OUTPUT FILTER	.99	1.0	0.50	0.10	0.10	0.50
FIVE VOLT OUTPUT RECTIFIER		-	2.00	0.40	0.40	2.00
TWENTY VOLT OUTPUT RECTIFIER		-	0.5	0.10	0.10	0.50
FIVE VOLT OUTPUT PERCENT REGULATION				0.90	2.65	4.50
TWENTY VOLT OUTPUT PERCENT REGULATION				0.60	2.35	3.00

The fifty percent load change for the distributed AC system is reflected through the main inverter transformer and the individual load change of ten percent is reflected through the remaining functional elements of the transformer-rectifier. Note that these are the same as that portion of the DC to DC converter. These are tabulated and totaled in the distributed AC column.

The distributed DC system provides a two to one improvement in regulation over the distributed AC system, reducing the requirement for post regulators.

Electromagnetic Control

Electromagnetic control is design practice to minimize malfunctions or performance degradation due to generated electromagnetic interference (EMI).

Single point grounding is considered a system requirement. Both the distributed DC and AC systems allow load isolation where current paths are easily controlled and where single point grounding is possible. The centralized DC system, however, assures conductive coupling between loads.

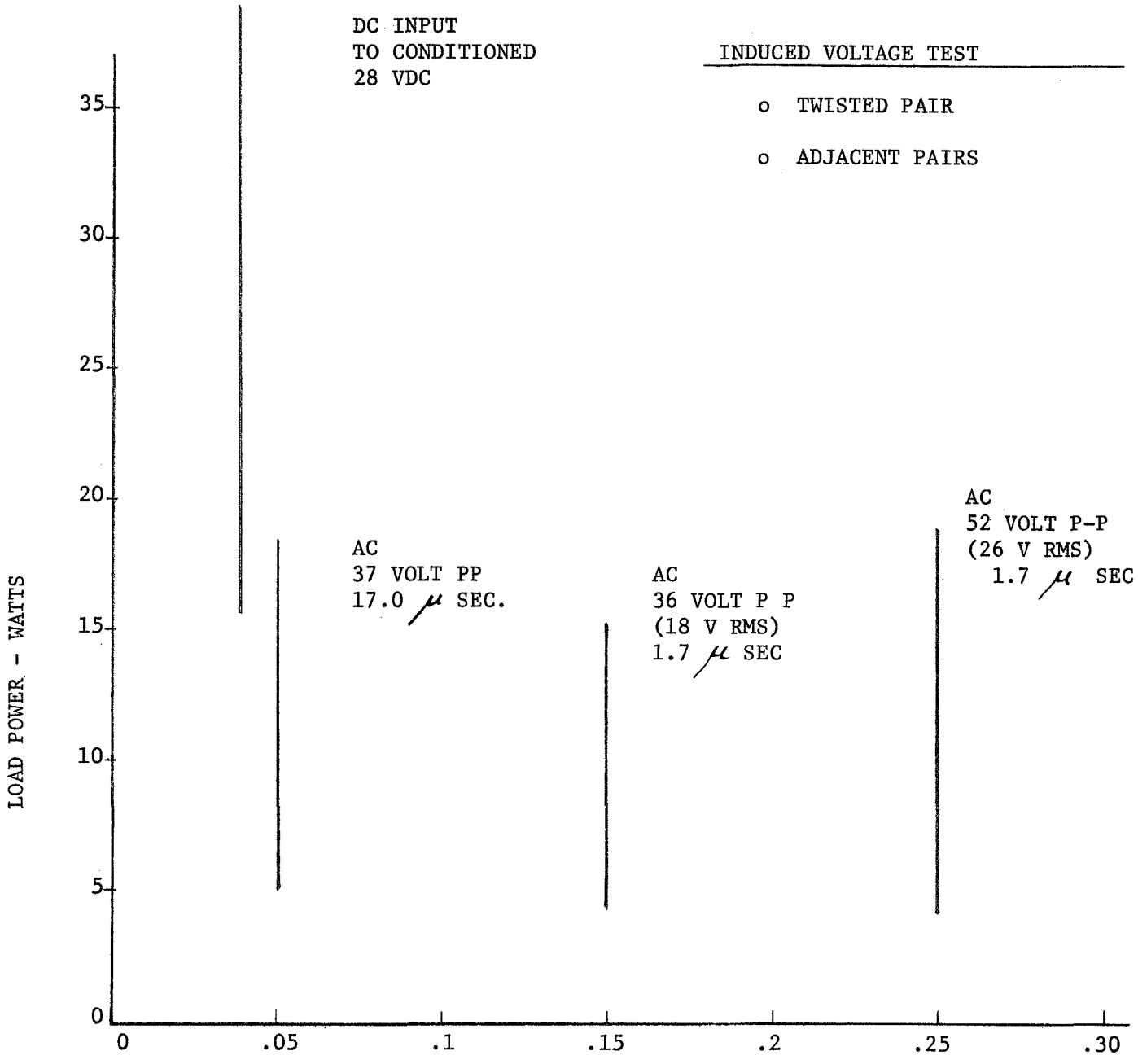
Compatibility within a subsystem can be demonstrated with a single subsystem test. Both the distributed DC and AC systems permit complete and separate subsystem testing with margins. The centralized DC system requires complete electrical system testing to verify compatibility between subsystems because of the common power supply. Further, actual margins for the centralized DC system are difficult to identify. For these reasons, the centralized DC system is considered least desirable from the EMC standpoint.

DC isolation is provided by both the distributed DC and AC systems. The electrical noise produced with highly efficient DC to DC converters or inverters is at radio frequency, and isolation is desirable, particularly for a spacecraft having an AC magnetometer. The distributed DC system provides additional filtering between subsystems due to both input and output filtering; and because the noise generating circuits (oscillator, power switch and transformers) are in close proximity to each other. By contrast, the distributed AC system distributes the switching noise throughout the spacecraft.

Noise tests were performed to obtain a relative indication of relative coupling. Figure 7-32 is a copy of some results. The following observations are made:

- o induced voltage for AC system is a function of voltage and rise time.
- o induced voltage is independent of power.
- o induced voltage is greater for the AC system.

For these reasons the DC system is preferred.



INDUCED VOLTAGE RESULTS

Figure 7-32

Producibility

The number of different power conditioning units that must be provided is a measure of the cost through the design, development, manufacturing, type approval, integration, and system test phases.

For the distributed AC system 32 transformer-rectifier units are required, since each will be designed to satisfy a specific load requirement. In addition, a main inverter will be required.

For the distributed DC system 32 DC to DC converters are required. These may be viewed as 32 transformer-rectifiers with individual inverters (the power oscillator for the DC to DC converter). A review of loads suggests five possible levels; therefore, five different inverters are required. The addition of one of the five inverters to a transformer-rectifier results in 32 DC to DC converters.

For the centralized DC system only one design is required. However, the selection of load voltages to be furnished will require some load redesign. Assuming load redesign and no serious load changes, the centralized DC system is most desirable in that only one unit is required, but integration and test may be costly due to design changes and the extensive test procedures to assure system compatibility.

Both the distributed DC and AC systems require equal integration and test since both contain an equal number of units. However, the distributed AC system is preferred since only one inverter design must be developed compared with the five for the distributed DC system. After the development phase, the costs of the two systems should become equal.

Switching

A critical portion of the power distribution system is the control of loads through switching. Magnetic latching relays for power switching are efficient and reliable for many cycles of operation. By comparison, static switching is less efficient but could be more reliable by careful design of the switching circuitry.

Relays in a redundant configuration are being considered, and for both the distributed DC or AC system the number of relays is identical and provides equal efficiency and size. However, static switches for the distributed AC system are different from the DC and result in unequal efficiency and size. The following is a comparison of AC and DC static switches.

Desirable system operation considerations which could be implemented as part of the switch circuitry are:

- static switching
  "on" high efficiency
  "off" low standby power
- turn on transient control
  peak current - 125 percent of nominal
- fault current limit
- fail safe operation

TABLE 7-11

STATIC SWITCH COMPARISON

SWITCH	DC	AC
Efficiency	.995	.98
Size:		
Switch Wt.	.1 Lb.	.32 Lb.
System Wt. *	3.2 Lb.	10.5 Lb.
Switch Size	1.3 in ^{3}	2x Power Trans
Reliability **		
Command	High	High
Circuit Comp.	Higher	
Comp. Count	Higher	

* Based on 10 Watt load average.

** Requires additional effort for further reliability evaluation.

The design concepts reviewed are shown in Figure 7-33. The AC static switch is a saturable reactor. Switch action is controlled through excitation of bias windings. Turn-on transient control and fault current limiting is inherent in its constant current characteristics. Fail safe operation for faults downstream of the switch is provided since the switch fails in the conducting state. A back-up switch is required for loads that must be switched off for power control. A relay is a good candidate for this application since it provides functional redundancy.

A DC static switch candidate is the DC to DC converter power transistors which are base controlled by auxiliary reverse voltage. Turn-on transient control and fault current limiting is provided by a magnetic amplifier that also applies an off voltage to the switching transistors when the input current is above the prescribed value. Additional turn-on transient control is through the design of the LC input filter. Fail safe operation is confined to load faults downstream of the switch. In the event of switch failure, fault protection such as a fuse or circuit breaker is required.

For fail safe comparison purposes the AC switch continues to provide the same average current to the load; and a relay is suggested for back-up load removal. A DC switch failure could provide the same average current or a very high current demand, and a fuse or circuit breaker is required.

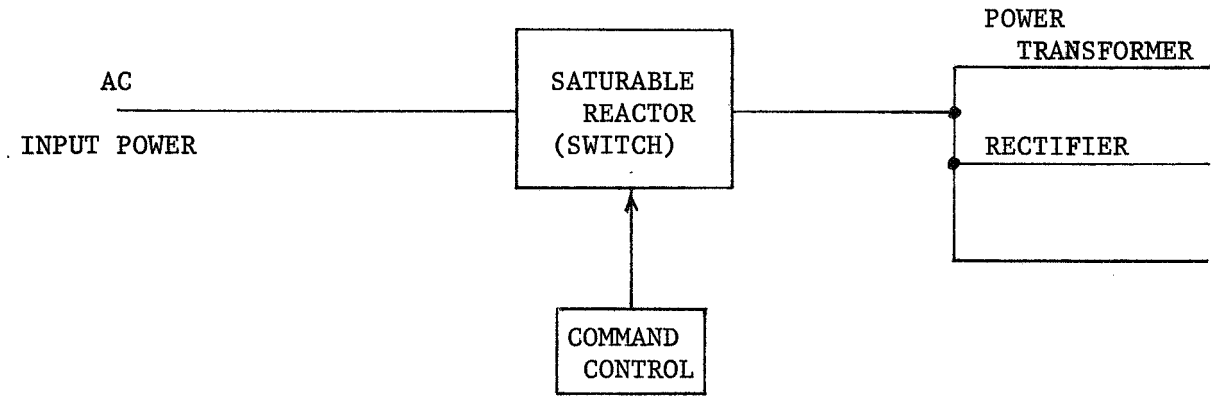
This analysis assumed relay back-up to static switching and a fuse for fault removal for the distributed DC system. Relay weight was not included since it is common to both systems. Fuse weight is included as part of associated electronic piece parts for the DC static switch.

The results are summarized in Table 7-11. The efficiency for the distributed DC system is based on bias power requirements for current limiting. The efficiency for the distributed AC system is based on bias power and copper loss only, since little core loss occurs during the 'bn' period. The standby power for "off" periods is considered equal for both systems considered. The weight is based on a ten watt average load. The distributed AC system switch weight by definition is greater than the size of the power transformer, since in the "off" condition it must support full voltage and present minimum series resistance. The DC switch weight is the weight of a low power magnetic amplifier and transistor switches. Presently the complexity and parts count for the DC static switch is greater, but a detailed reliability analysis must be performed on the actual circuits.

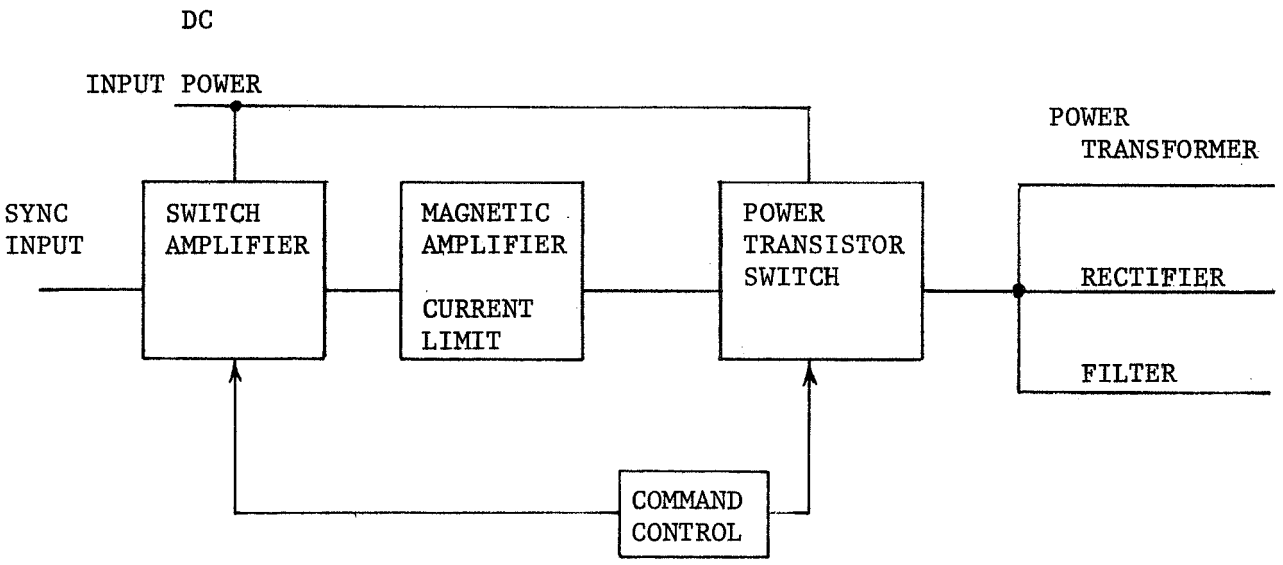
The DC system appears to have higher efficiency and lower weight, but the difference between systems is not conclusive on reliability considerations.

Conclusion

The centralized DC system provides the highest efficiency and lowest electronic piece part count when it is used for a single load. However, where a large number of loads are cycled the system is complicated by a large increase in relays and relay driver circuits. In addition, the interaction at the power supply is difficult to verify at the subsystem level. This system is not recommended for further consideration.



DISTRIBUTED AC CONCEPT



DISTRIBUTED DC CONCEPT

STATIC SWITCH CONCEPTS

Figure 7-33

Comparing the quantitative results of the distributed AC and DC systems shows that no parameter by itself can greatly influence the selection. However, a greater number of advantages appear for the distributed DC system and it is recommended for further development for TOPS. This recommendation is based on:

- o reliability - growth is possible at lower stress levels
- o decentralization provides greater fault removal capability
- o higher efficiency
- o lower noise coupling
- o load isolation

Additional recommendations are to continue to investigate and solve detail design problems for both distributed AC and DC systems, but concentrate on the distributed DC approach, to investigate various static switching methods, and to establish interface control procedures.

7.3 Electronic Piece Part Failure Rate

Information provided by the Jet Propulsion Laboratory in Technical Direction Memorandum No. TOPS-69-101 dated 26 September 1969 and shown in Table 7-12 is the failure rate data for electronic piece parts that will be used during all subsequent work for relative reliability. The only significant change from data used during the first quarter and shown in Table 7-1 of the First Quarterly Technical Report 1J86-TOPS-479 dated 15 October 1969; and from data used in the analyses reported herein and shown in Table 7-9 is the addition or different interpretation of failure rates on electromagnetic devices.

Table 7-12

Recommended Part Failure Rate Data

Part Type	Failure Rate x 10^{-6} failures per hour
Capacitors	
Glass	.002
Ceramic	.005
Foil	.008
Tantalum	
Solid	.01
Wet	.1
Diodes	
Signal & Switching	.01
Zener	.02
Power	.05
Resistor	
Carbon Composition	.001
Film	.008
Wire Wound	.09
Transistors	
Small Signal bi-polar	.02
Power Bi-polar	.08
JFET	.02
Isolated Gate FET	.05
Silicon Controlled Rectifier/Switch	.07
I/C's (does not include MSI/LSI)	
Bi-polar Monolithic	.2
MOS Monolithic	.4
Relays (Mech)	2.0
Transformer	
Saturable	.006 per winding
Low Voltage	.018 per winding
High Voltage	.10 per winding
Inductor	.01

7.4 Shunt Regulator Reliability Analysis

Introduction

Two basic shunt regulator configurations were compared with respect to failure modes and effects and relative numerical reliability. The central reference with multiple shunts, shown in Figure 7-34 was judged less desirable than the quaded reference and shunt, shown in Figure 7-35. The results of the numerical reliability comparisons are presented in Figure 7-43.

Multiple Shunts

Figure 7-34 shows the basic concept for a multiple shunt system. The redundant central reference and control circuit is switched to backup automatically by a failure detector so that no failure maintains an over or under voltage condition on the bus. Figure 7-36 shows the circuit which would be used for reference and Figure 7-37 shows the schematic of an over-under voltage failure detector and switchover circuit. The capacitor C1 provides energy storage to assure switchover despite a failure which could result in an instantaneous drop of the bus voltage to a low value. Figure 7-38 is the schematic of a shunt element. R1 and R2 are power resistors for reducing power dissipation in Q1 and Q2. For a low number of shunts (~ 8), Q1 and Q2 would be large power transistors (high power shunt), but if many shunt ($\geqslant 10$) were to be used, Q2 could be a medium power transistor and R2 can be eliminated (low power shunt).

Table 7-13 lists the parts and corresponding failure rates for the above circuits. The failure rates are taken from Table 7-1 of the First Quarterly Technical Report 1J86-TOPS-479 dated 15 October 1969. The reliability model and associated mathematics for calculating a probability of success for multiple shunt configuration is given in Figure 7-39. The binomial probability is used in calculations for the shunts since failure, particularly opens, can be tolerated with proper load manipulation. The mathematics of the model is contained in a desk side computer program MULTSREL shown in Table 7-14. For analyzing just the binomial probabilities of many elements allowing failures, a second program TJEPLREL, shown in Table 7-15, was used.

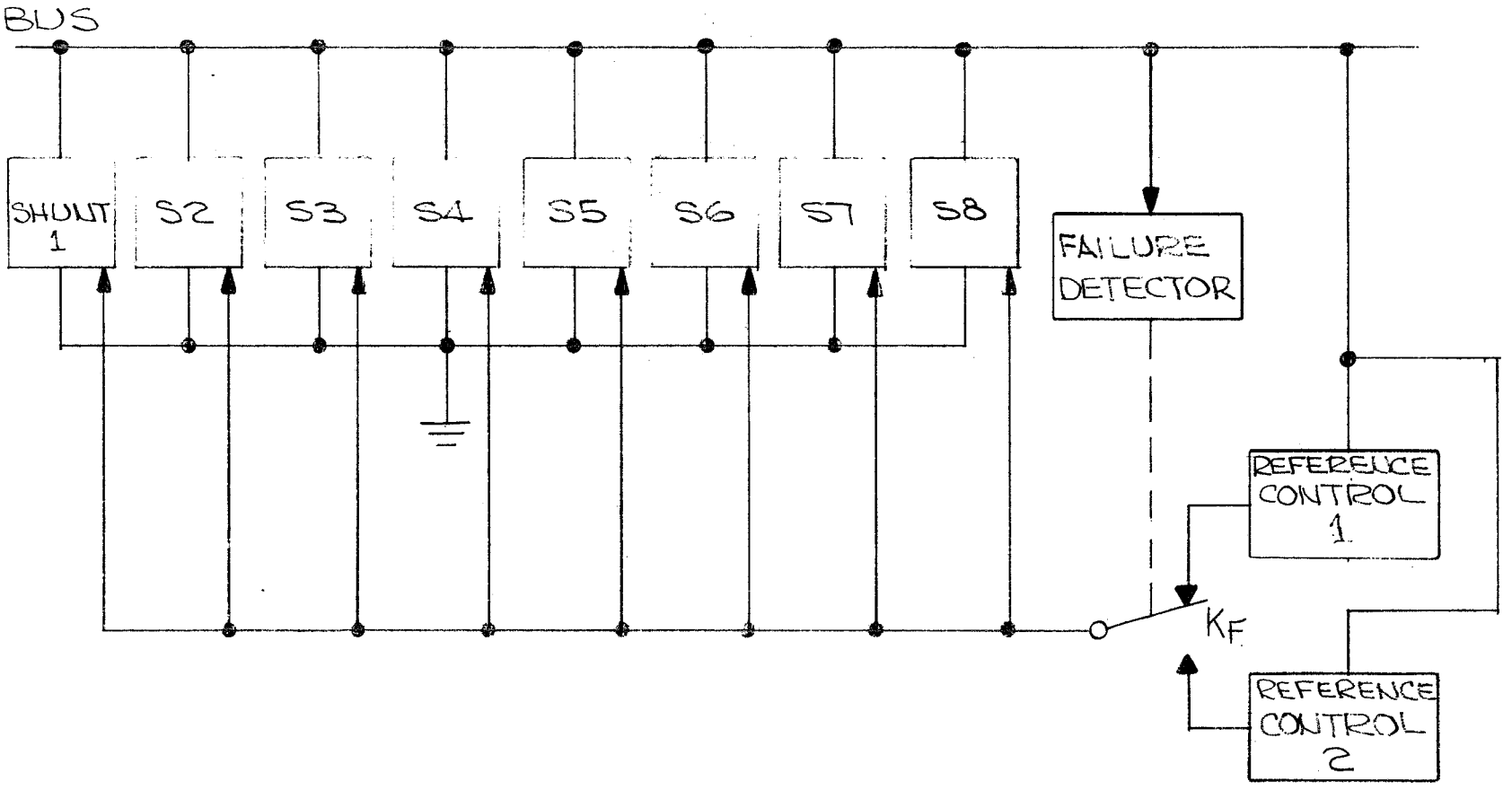


Figure 7-34. Multiple Shunt Configuration

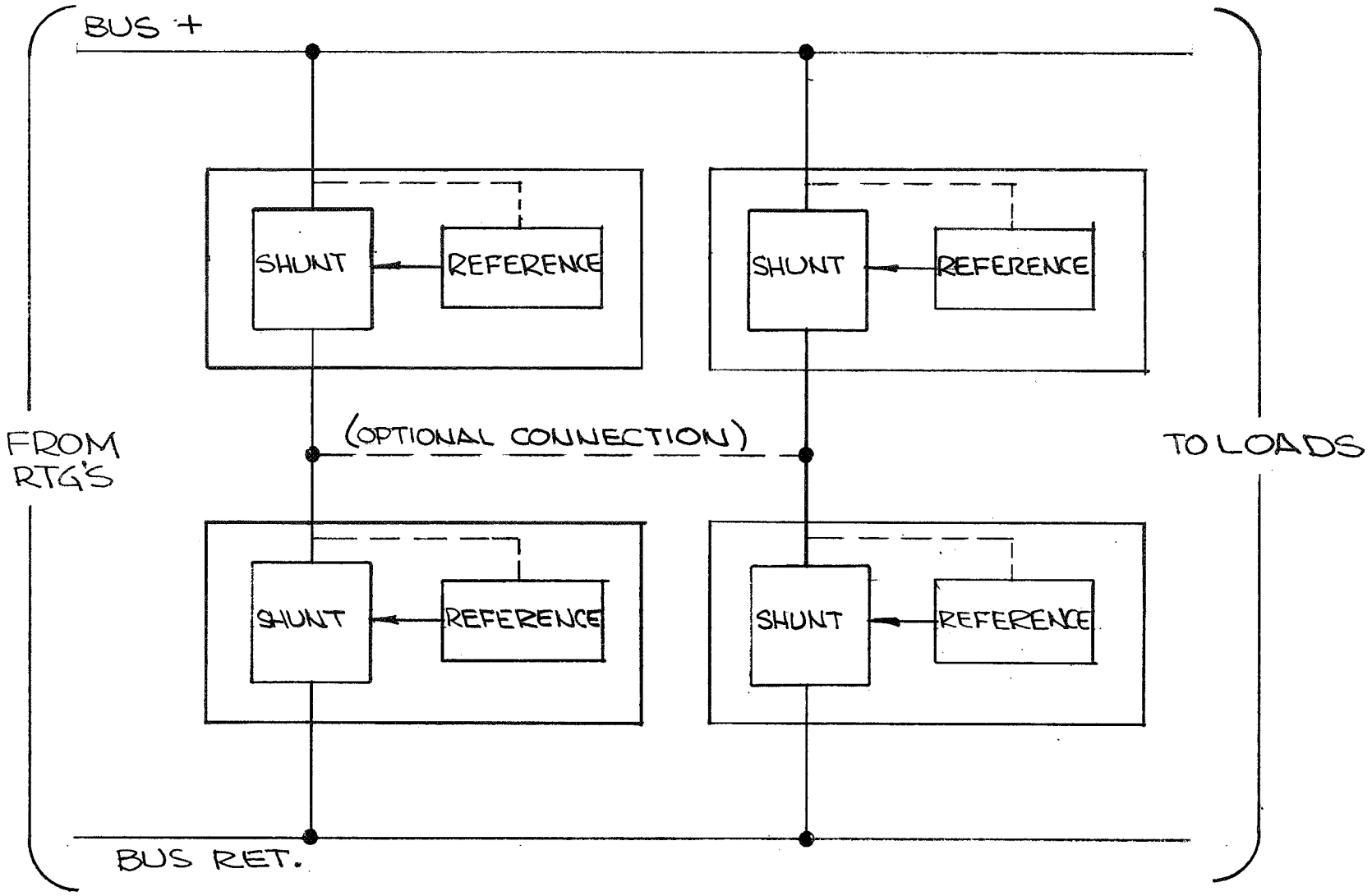


Figure 7-35. Quad Redundant Shunt Configuration

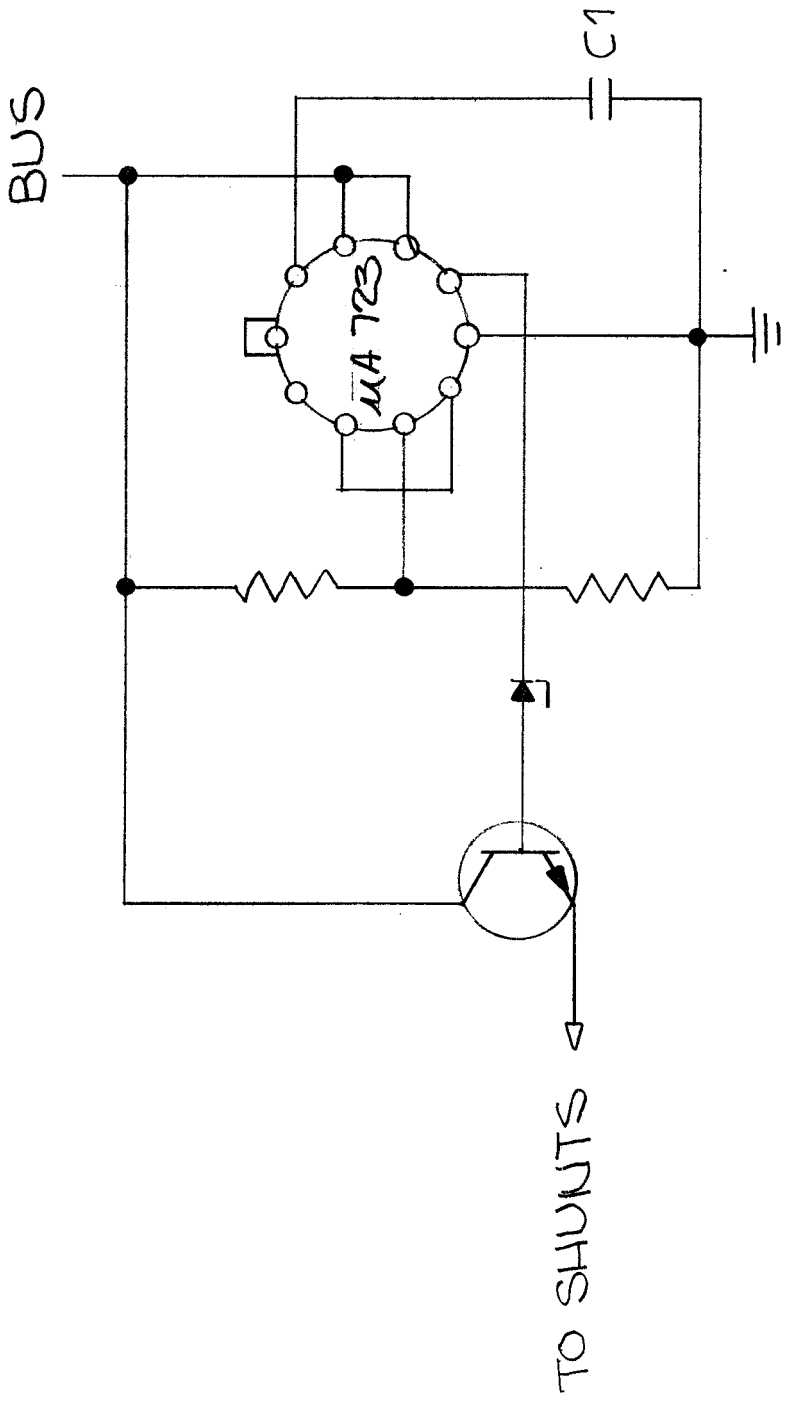


Figure 7-36. Multiple Shunt Driver Schematic

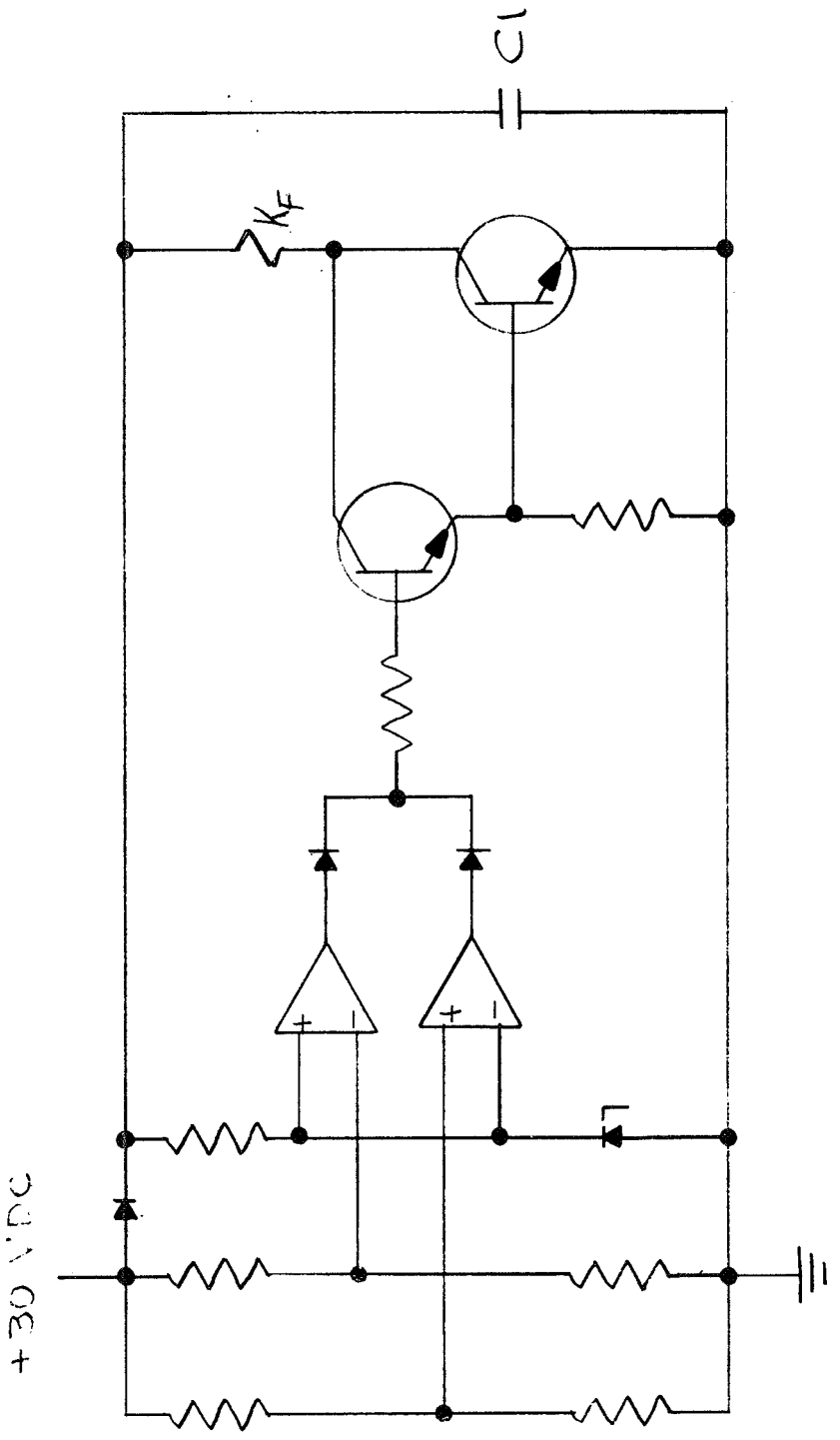


Figure 7-37. Shunt Regulator Failure Detector

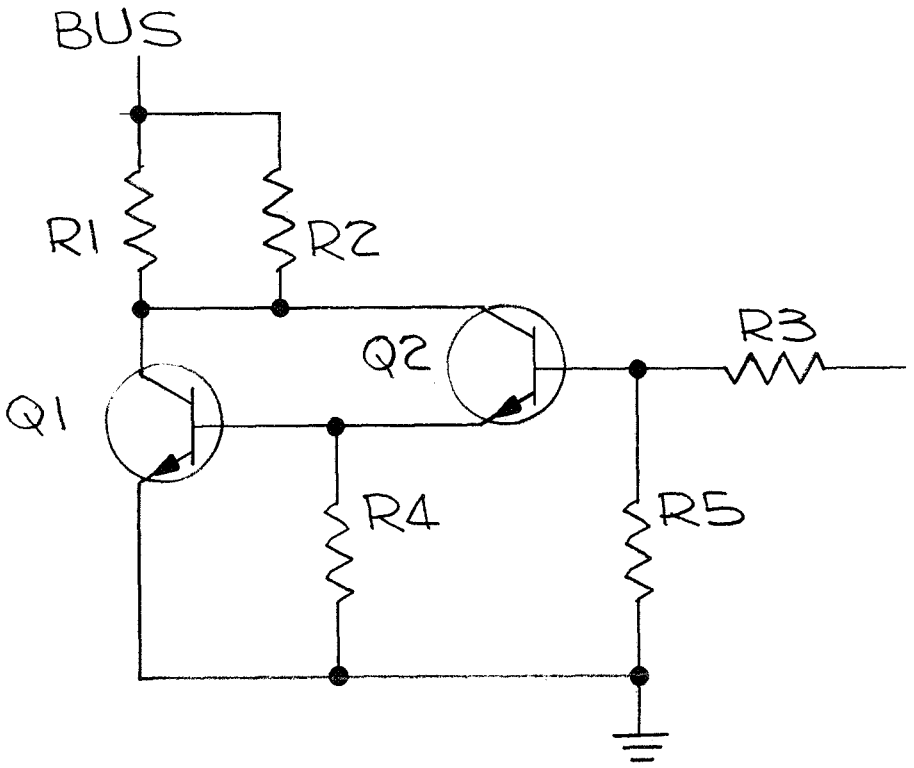


Figure 7-38. Single Element of a Multiple Shunt Regulator

Table 7-13. Shunt Regulator Piece Part Failure Rates

Piece Part Failure Rate/10^6 hrs.	Power Resistor .09	Film Resistor .008	Power Transistor .08	Signal Transistor .02	J FET .02	Ceramic Capacitor .005	Foil Capacitor .008	Zener .02	Signal Diode .01	I.C. .2	Relay 2.	Total/10^6 Hrs.
High Power Shunt	2	1	2									.348
Low Power Shunt	1	1	1	1								.198
Shunt Driver		2		1				1		1		.256
Failure Detector		7		2			1	1	3	1	1	2.35
Quad Elements (↗Open)		3	4 (10%)					1		1 75%		.226
Quad Elements (↗Short)		1	4 (90%)							.1 25%		.346

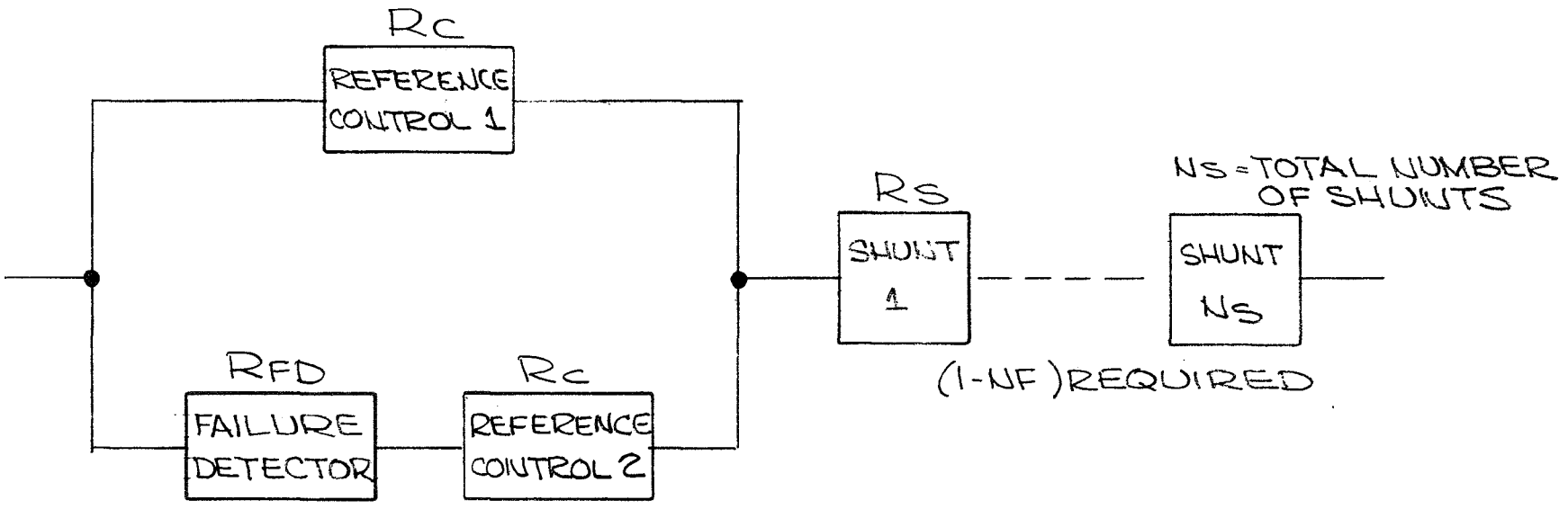


Figure 7_39. Multiple Shunt Regulator Reliability Model

Table 7-14. MULTSREL Computer Program

```
00010 * CALCULATES RELIABILITY FOR MULTIPLE SHUNT SCHEME
00020 PRINT:"    MISSION TIME (YEARS)";READ:TY
00030 9 PRINT:" "
00040 PRINT:" ELEMENT LAMBDA, NUMBER OF SHUNTS, NUMBER OF SHUNT
00050 &FAILURES";READ:YS,NS,NF
00060 IF(YS.EQ.0.)STOP
00070 T=-TY*365.25*24.0*1.0E-06
00080 PRINT:"   CONTROL, FAILURE DETECTOR LAMBDAS";READ:YC,YFD
00090 RC=EXP(YC*T);RFD=EXP(YFD*T)
00100 R1=RC+RC*RFD-RC*RC*RFD
00110 31 CONTINUE
00120 RS=EXP(YS*T)
00130 PRINT 102,RS
00140 PRINT 103,RC,RFD
00150 PRINT 100
00160 FACT=1.;I=0;POW=1.
00170 RT=RS**NS;R=RT
00180 PRINT 101,I,R
00190 DO 10 I=1,NF
00200 FACT=FACT*(NS-I)/I
00210 RT=RT+FACT*(1-RS)**I*RS**(NS-I)
00220 R=RT*R1
```

Table 7-14. MULTSREL Computer Program (Continued)

```
00230 10 PRINT 101,I,R
00240 PRINT:" ";PRINT:" ";GO TO 9
00250 100 FORMAT(1H-,"NUMBER ALLOWED",/,1H ,"   TO FAIL",
00260 &14X,"RELIABILITY")
00270 101 FORMAT(1H ,I13,F20.7)
00280 102 FORMAT(1H0,"SHUNT RELIABILITY=",F10.6)
00290 103 FORMAT(1H ,"CONTROL RELIABILITY=",F10.6,/,1H ,
00300 &"FAILURE DETECTOR RELIABILITY=",F10.6)
00310 END
END OF FILE MULTSREL
```

Table 7-15. TJEPLREL Computer Program

```
00010 PRINT:" MISSION TIME IN YEARS";READ:TY
00020 TIM=-TY*365.25*24*1.0E-06
00030 PRINT:" ELEMENT LAMBDA, FAILURES PER MILLION HOURS";READ:YRES
00040 RRES=EXP(YRES*TIM)
00050 PRINT:" ELEMENT RELIABILITY=";PRINT 102,RRES
00060 PRINT:" NUMBER"
00070 PRINT:"    IN"
00080 PRINT:" PARALLEL    NUMBER ALLOWED TO FAIL"
00090 PRINT:"     '          0          1          2          3
00100 &          4"
00110 PRINT:"     '          5          6          7          8
00120 &          9"
00130 DO 21 NRES=2,15 ; PRINT 101,NRES
00140 NF=NRES-2
00150 IF(NRES.GT.11)NF=9
00160 RTRES=EXP(NRES*YRES*TIM)
00170 PRINT 102,RTRES
00180 IF(NF.EQ.0)GO TO 21 ; FACT=1
00190 DO 23 I=1,NF
00200 FACT=FACT*(NRES-I)/I
00210 20 RTRES=RTRES+FACT*(1-RRES)**I*RRES**(NRES-I)
```

Table 7-15. TJEPLREL Computer Program (Continued)

```
00220 IF(I.EQ.5)PRINT 103,NRES
00230 23 PRINT 102,RTRES
00240 22 CONTINUE ; 21 CONTINUE
00250 STOP
00260 101 FORMAT(1H0,I5)
00270 102 FORMAT(1H&,F12.7)
00280 103 FORMAT(1H ,I5)
00290 END
END OF FILE TJEPLREL
```

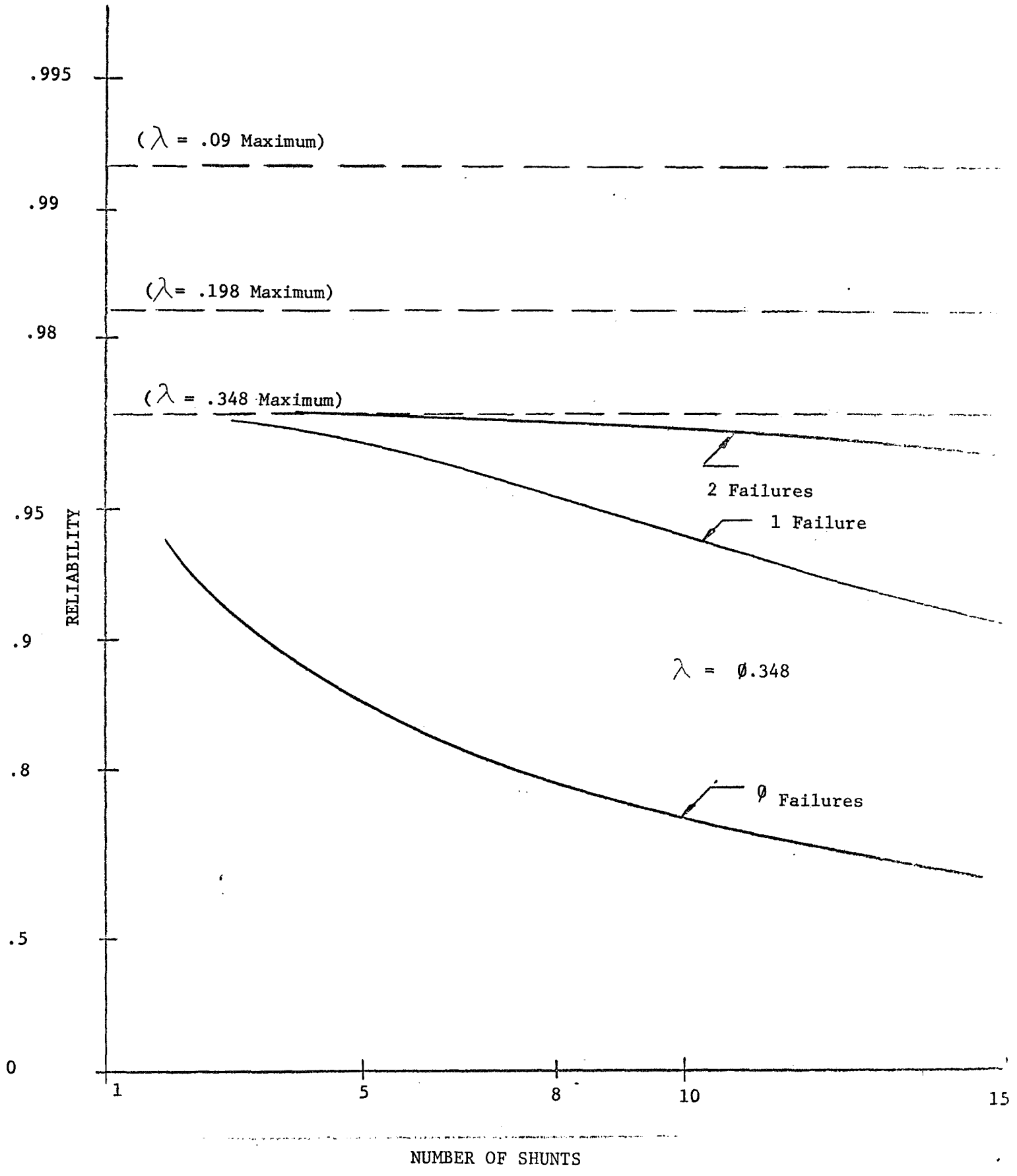


Figure 7-40. Multiple Shunt Reliability

Table 7-16 shows the results of executing MULTSREL for the configuration being discussed. The probabilities of success allowing 0, 1 or 2 failures is printed. The top printout gives the probabilities for the system as discussed, the lower printout calculates the probabilities with control and failure detector reliabilities of 1. The small difference (.9691 versus .9647 at 2 failures) shows that the major contributor to the unreliability, especially where fewer than two failures are allowed, is the shunts, not the control or failure detector.

To be realistic, the multiple shunt system would absorb some shunt elements failed open with no effect on regulation due to design margins. Figure 7-40 presents the reliability of just the shunts, the results of executing TJEPLREL, shown in Table 7-16. Allowing two failures provides nearly maximum reliability from 4 to 10 shunts, and little under the maximum for 10 to 15 shunts, as can be seen from the λ = .348 curve. The 1 and 0 failure curves show the great reduction in reliability for more than 8 shunts when fewer failures can be tolerated. To assess the maximum possible reliability that could be obtained from a multiple shunt system, it was assumed that only failures short would be counted in a system of 8 or more low power shunts. Accordingly, only two transistors could contribute to a short failure because it is assumed that a resistor cannot fail in such a manner as to cause overdrive of the shunt. In addition, it was assumed that 10% of the transistor failures would be open. Therefore, the probability of a shunt failure would be $\frac{.9\ \lambda \text{ transistors}}{\lambda \text{ total}}$ where R-e- λ total x time. For an approximation this was assumed to be

$1-e^{-.9\ \lambda \text{ transistor x Time}}$ to facilitate input to the program.

Accordingly, the lower printouts of Table 7-17 shows an element λ of .09, (.9 X (.08 + .02)). Under these assumptions, every failure would correspond to a power loss corresponding to V^2/R; where V = bus voltage and R is the value of the shunt power resistor. If one failure short can be tolerated, the reliability would be .986 using the 8 shunt printout, and .982 for 15 shunts.

Quaded Reference-Shunts

The general configuration for the quad shunt proposed for TOPS is given in Figure 7-35. The detailed schematic of the shunt is included in Section 4. Two configurations were examined, an H configuration and a II configuration, that is, center connected and center not connected.

Obviously this system can absorb one or more failures with no effect on regulation. It is likewise evident that how the element fails determines the effect. Referring to Figure 7-35, a short in either top element and short in either bottom element would short the bus, but two opens in the same place have no effect. Accordingly, a different approach to the analysis was used.

Table 7-16. Multiple Shunt System Reliability

```
$FORT MULTSREL

    MISSION TIME (YEARS)=10

 ELEMENT LAMBDA, NUMBER OF SHUNTS, NUMBER OF SHUNT FAILURES=0.348, 8, 2

   CONTROL,FAILURE DETECTOR LAMBDAS= 0.256, 2.345


SHUNT RELIABILITY=  0.969955
CONTROL RELIABILITY=  0.977809
FAILURE DETECTOR RELIABILITY=  0.814189


NUMBER ALLOWED
   TO FAIL              RELIABILITY
         0              0.7834520
         1              0.9490150
         2              0.9647297


 ELEMENT LAMBDA, NUMBER OF SHUNTS, NUMBER OF SHUNT FAILURES=0.348, 8, 2

   CONTROL,FAILURE DETECTOR LAMBDAS= 0.0, 0.0


SHUNT RELIABILITY=  0.969955
CONTROL RELIABILITY=  1.000000
FAILURE DETECTOR RELIABILITY=  1.000000


NUMBER ALLOWED
   TO FAIL              RELIABILITY
         0              0.7834520
         1              0.9533281
         2              0.9691142


 ELEMENT LAMBDA, NUMBER OF SHUNTS, NUMBER OF SHUNT FAILURES=0,0,0


PROGRAM STOP AT 60

READY
```

Table 7-16. SHUNTREL Computer Program

```
00010 DIMENSION T(6,6),S(6),SX(6)
00020 ASCII AX(10),DATE(2)
00030 CALL DATE#TIM(DATE,HOUR)
00040 PRINT 107,DATE,HOUR; 107 FORMAT(1H ,2A4,F7.3)
00050 PRINT:" MISSION TIME IN YEARS";READ:TY
00060 TIM=-TY*365.25*24*1.0E-06
00070 PRINT:"  TYPE IN LAMBDAS IN FAILURES PER MILLION HOURS"
00080 PRINT:"      RESISTOR,SHUNT(OPEN),SHUNT(SHORT)";READ:YRES,YSO,YSS
00090 RRES=EXP(YRES*TIM)
00100 PRINT:" NUMBER RESISTORS IN PARALLEL, NUMBER ALLOWED TO FAIL"
00110 READ:NRES,NF
00120 PRINT:"  QUAD CENTER CONNECTED?"; READ:AX(1)
00130 RTRES=EXP(NRES*YRES*TIM)
00140 IF(NF.EQ.0)GO TO 21 ; FACT=1
00150 DO 20 I=1,NF
00160 FACT=FACT*(NRES-I)/I
00170 20 RTRES=RTRES+FACT*(1-RRES)**I*RRES**(NRES-I)
00180 21 R1=RTRES*RTRES ; PRINT 101,R1
00190 TK=TIM/1000
00200 RS=EXP(TK*(YSS+YSO))
00210 QO=YSO/(YSS+YSO)*(1-RS)
00220 QS=YSS/(YSS+YSO)*(1-RS)
00230 DO 22 I=1,6
```

Table 7-16. SHUNTREL Computer Program (Continued)

```
00240 T(I,6)=1;S(I)=0
00250 DO 22 J=1,5
00260 22 T(I,J)=0.
00270 S(1)=1.000
00280 *  TRANSITION MATRIX ELEMENTS CALCULATION*******
00290 T(1,1)=RS*RS*RS*RS
00300 T(1,2)=2.*QS ; T(1,4)=2.*QS
00310 T(1,3)=2.*QQ ; T(1,5)=2.*QQ
00320 T(2,2)=RS*RS ; T(2,5)=2.*QQ
00330 T(3,2)=QS ; T(3,3)=RS*RS*RS
00340 T(3,4)=2.*QS ; T(3,5)=2.*QQ
00350 T(4,3)=2.*QQ ; T(4,4)=RS*RS
00360 T(5,2)=2.*QS ; T(5,3)=2.*QQ
00370 T(5,4)=QS ; T(5,5)=RS*RS*RS
00380 IF(AK(1).EQ."YES") GO TO 28
00390 T(2,2)=RS*RS*RS; T(2,3)=QQ; T(2,4)=2.*QS
00400 T(3,2)=0.; T(3,3)=RS*RS; T(5,4)=0.; T(5,5)=RS*RS
00410 T(4,2)=2.*QS; T(4,4)=RS*RS*RS; T(4,5)=QQ
00415 T(3,5)=0. ; T(5,3)=0.
00420 28 CONTINUE
00430 DO 23 I=1,5
00440 DO 23 J=1,5
00450 T(I,6)=T(I,6)-T(I,J)
```

Table 7-16. SHUNTREL Computer Program (Continued)

```
00460 23 IF(T(I,6).LT.0)T(I,6)=0.
00470 T(6,6)=1
00480 PRINT 103,-TX*1.0E+06,(I,I=1,6)
00490 DO 24 I=1,6
00500 24 PRINT 102,I,(T(I,J),J=1,6)
00510 Y=0. ; NX=1 ; PRINT 105,(NI,NI=1,6)
00520 PRINT 104,Y,(S(I),I=1,6)
00530 DO 25 N=1,1000
00540 DO 26 J=1,6
00550 SX(J)=0.
00560 DO 26 I=1,6
00570 26 SX(J)=SX(J)+S(I)*T(I,J)
00580 DO 27 L=1,6
00590 27 S(L)=SX(L)
00600 Y=Y-TX*1.0E+06/365.25/24
00610 IF(N.EQ.(NX-1))PRINT 104,Y,(S(I),I=1,6)
00620 IF(N.EQ.NX)NX=NX+100
00630 25 CONTINUE
00640 R=(S(1)+S(2)+S(3)+S(4)+S(5))*R1
00650 PRINT 106,R
00660 101 FORMAT(1H-,' RESISTOR BANK RELIABILITY=',F11.6)
00670 102 FORMAT(1H ,I3,6F11.8)
```

Table 7-16. SHUNTREL Computer Program (Continued)

```
00680 103 FORMAT(1H-,"     TRANSITION MATRIX FOR",F8.3," HOURS",/,
00690 &1H ,7X,6(I2,9X))
00700 104 FORMAT(1H0,F5.2,6F10.6)
00710 105 FORMAT(1H-,"        STATE MATRIX",/,1H ," YRS",4X,6(I2,8X))
00720 106 FORMAT(1H-,"     *****TOTAL OVERALL RELIABILITY=",
00730 &F10.7,"*****")
00740 STOP
00750 END
END OF FILE SHUNTREL
```

Table 7-17. Modified Multiple Shunt Reliability

```
    MISSION TIME (YEARS)=10

 ELEMENT LAMBDA, NUMBER OF SHUNTS, NUMBER OF SHUNT FAILURES=0.198, 8, 2

   CONTROL,FAILURE DETECTOR LAMBDAS= 0.256, 0\2.345


SHUNT RELIABILITY=  0.982793
CONTROL RELIABILITY=  0.977809
FAILURE DETECTOR RELIABILITY=  0.814189


NUMBER ALLOWED
   TO FAIL                RELIABILITY
            0             0.8703556
            1             0.9726036
            2             0.9781810


 ELEMENT LAMBDA, NUMBER OF SHUNTS, NUMBER OF SHUNT FAILURES= 0.09, 8, 2

   CONTROL,FAILURE DETECTOR LAMBDAS= 0.256, 2.345


SHUNT RELIABILITY=  0.992142
CONTROL RELIABILITY=  0.977809
FAILURE DETECTOR RELIABILITY=  0.814189


NUMBER ALLOWED
   TO FAIL                RELIABILITY
            0             0.9388353
            1             0.9864052
            2             0.9876365


 ELEMENT LAMBDA, NUMBER OF SHUNTS, NUMBER OF SHUNT FAILURES= 0.09, 15, 3

   CONTROL,FAILURE DETECTOR LAMBDAS= 0.256, 2.345


SHUNT RELIABILITY=  0.992142
CONTROL RELIABILITY=  0.977809
FAILURE DETECTOR RELIABILITY=  0.814189


NUMBER ALLOWED
   TO FAIL                RELIABILITY
            0             0.8883930
            1             0.9824405
            2             0.9874894
            3             0.9876494
```

First the resistor bank configuration was analyzed with the aid of the deskside program TJEPLREL which calculates probabilities allowing failures among many elements. Each parallel string was first considered independent and then the overall bank reliability is (R parallel string)^2. Figure 7-41 graphically shows the general results for a parallel string allowing up to two failures for a failure rate of 0.09 per million hours. It is obvious from the graph that a design permitting two failures for a string of 4 to 14 resistors achieves the maximum reliability and the resistor bank is so designed.

The reliability numbers for the quad shunt elements are calculated by successive multiplications of a state matrix [S] by a transition matrix [T] to get the next state matrix. Each of the four elements in the shunt is assumed to fail such that it provides too much shunting (short) or provides insufficient shunting (open). The states are defined in Table 7-18 for both H and Π configurations.

Several assumptions are made in developing the transition matrix, which is the matrix of probabilities of changing state. ($\Pi(1,3)$ is the probability of going from state 1 to state 3 .) The transition probabilities are calculated for a small time interval, therefore the probability of two failures occuring within the time period can be ignored. That is, Q^n terms for $N > 1$ will be assumed insignificant. Since the Q's which were calculated in these computations were in the order of 10^{-5}, Q^2 terms can safely be assumed to be insignificant compared to a Q^1 term. Thus the probability of going from state 1 (no element failures) to state 6 (regulation failure) is 0. No change in the element failure mode can occur, that is, the element will not open after failing short or become shorted after failing open. It was assumed that 90% of the transistor failures were short, 75% of the comparator integrated circuit would cause insufficient shunting, and that resistors only fail open. With the preceeding assumptions, parts or failures which would not positively fail the circuit, such as base-emitter leakage resistor opens, were ignored. Lambda to open and lambda to short, as given in Table 7-13, were calculated by summing the part failure rate or the percentage of the part failure rate which contributed to that mode of failure. Since shorting of the zener diode would not cause too much shunting because the control circuit would compensate, its entire failure rate was charged against λopen. The R and Q values were calculated per the following:

$$R = e^{-(\lambda_O + \lambda_S)\Delta t}$$

$$Q_O = \frac{\lambda_O}{\lambda_O + \lambda_S}(1 - R)$$

$$Q_S = \frac{\lambda_S}{\lambda_O + \lambda_S}(1 - R)$$

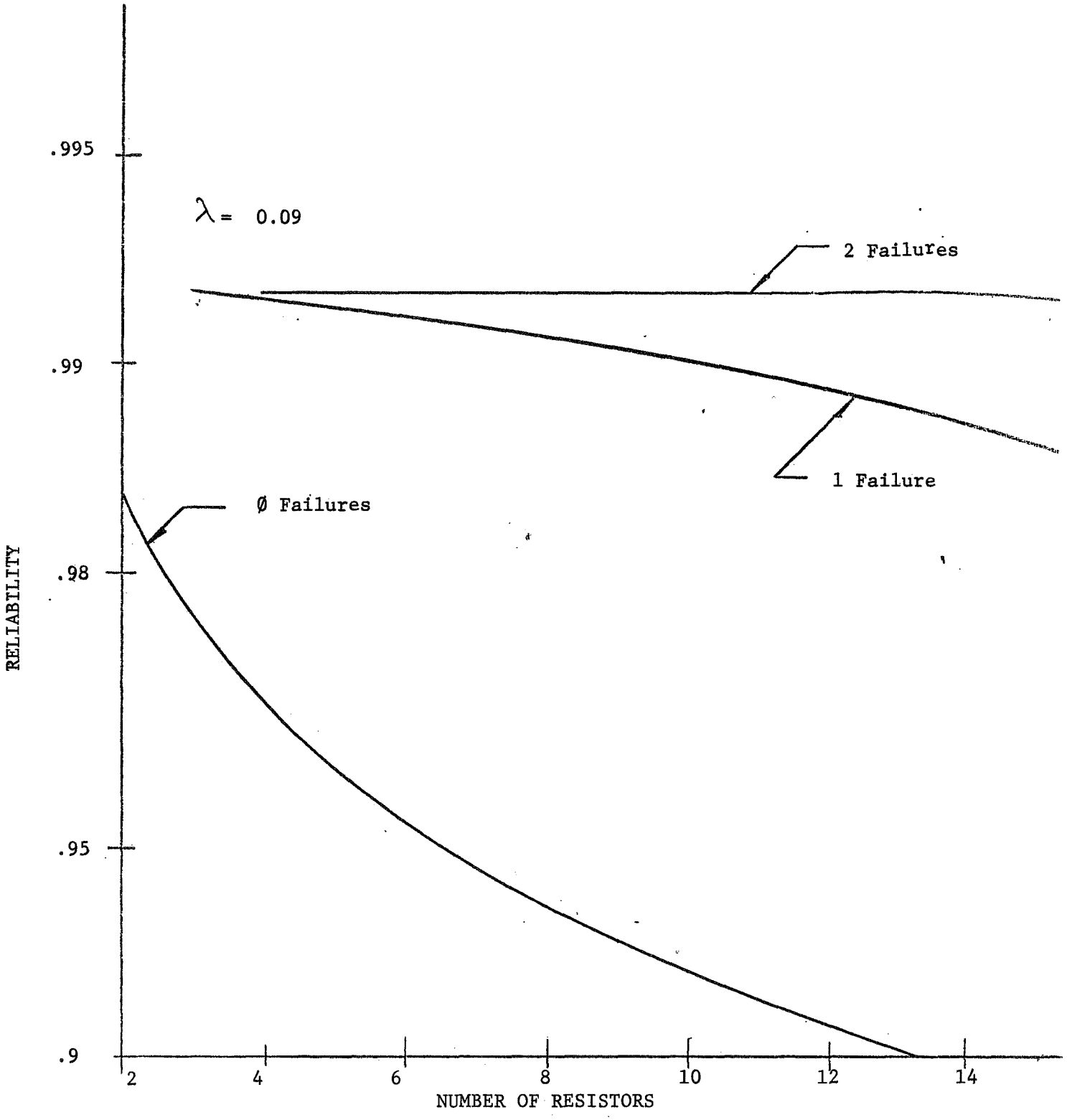


Figure 7-41. Resistor String Reliability

TABLE 7-18. State Definitions

Quad Center Connected

	TRANSITION MATRIX					
	1	2	3	4	5	6
1. No Element Failures	1. R^4	$2Q_s$	$2Q_o$	$2Q_s$	$2Q_o$	Ø
2. One of Top Shorted	2. Ø	R^2	Ø	Ø	$2Q_o$	1-others
3. One of Top Open	3. Ø	Q_s	R^3	$2Q_s$	$2Q_o$	1-others
4. One of Bottom Shorted	4. Ø	Ø	$2Q_o$	R_2	Ø	1-others
5. One of Bottom Open	5. Ø	$2Q_s$	$2Q_o$	Q_s	R^3	1-others
6. Bus Regulation Failure	6. Ø	Ø	Ø	Ø	Ø	1

Quad Not Center Connected

1. No Element Failures	1. R^4	$2Q_s$	$2Q_o$	$2Q_s$	$2Q_o$	Ø
2. One of Top Shorted	2. Ø	R^3	Q_o	$2Q_s$	$2Q_o$	1-others
3. One of Left Open	3. Ø	Ø	R^2	$2Q_s$	Ø	1-others
4. One of Right Shorted	4. Ø	$2Q_s$	$2Q_o$	R^3	Q_o	1-others
5. One of Right Open	5.					
6. Bus Regulation Failure	6. Ø	Ø	Ø	Ø	Ø	1

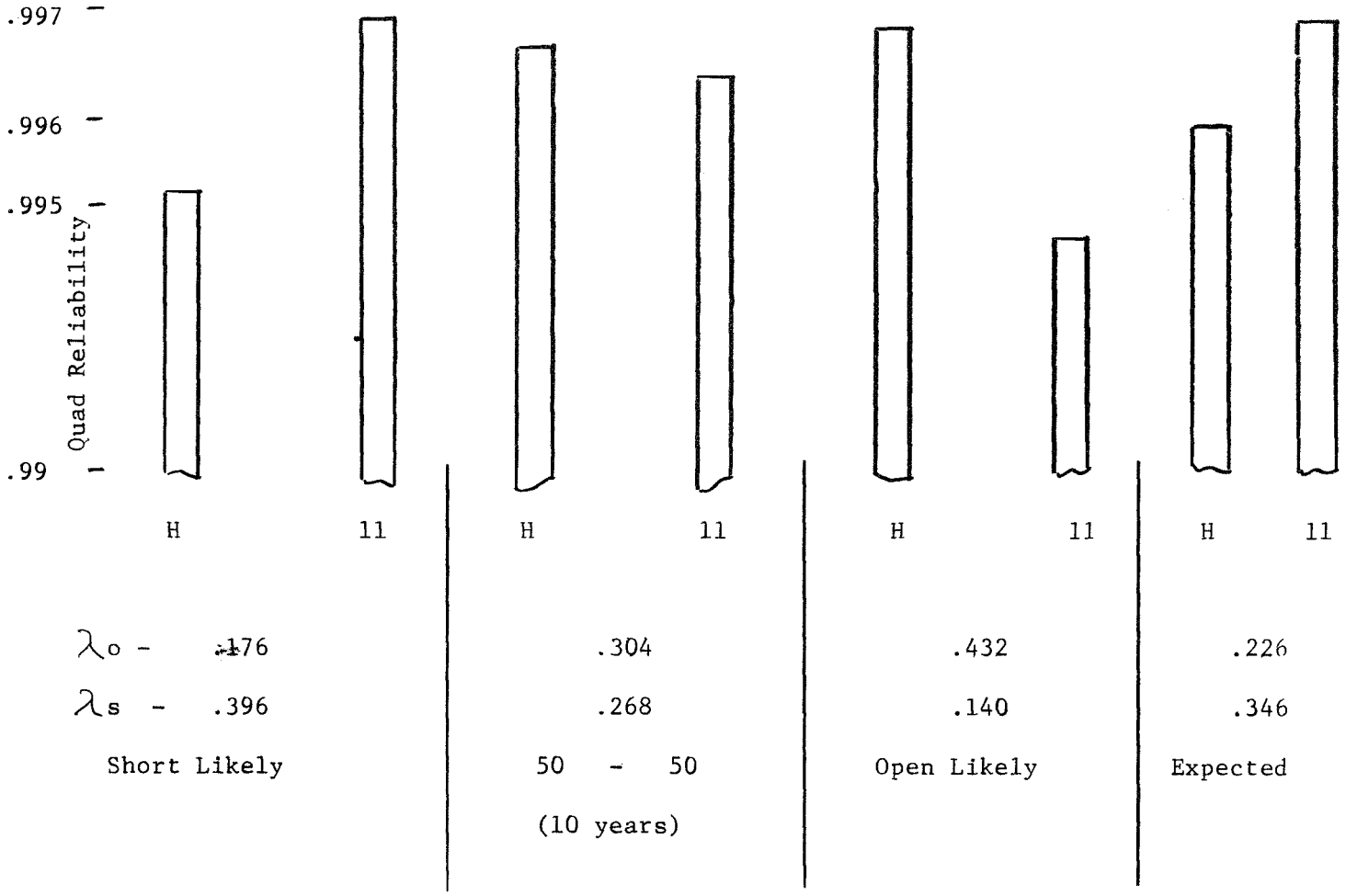


Figure 7-42. Shunt Regulator Comparative Reliability

A computer program was written for the deskside to handle the computations given below:

$$R_{SHUNT} = \left(\sum_{\chi=0}^{NF} \frac{NR!}{\chi!\ (NR-\chi)!}\ R_{RES}^{(NS-\chi)}\ (1-R_{RES})^{\chi} \right)^2 \times ([S] \times [T])^*$$

Where: NR = number of resistors in parallel
NF = number of resistors allowed to fail
R_{RES} = e - λ resistor x Time.

[S] = Quad state matrix
[T] = Quad transition matrix

* iterated 1000 times for any inputted total time.

The Program SHUNTREL calculates and prints out the resistor bank reliability, the 1000th time interval and corresponding transition matrix, and 10 state matrices so that the flow of state changes can be followed. A sample printout is given in Table 7-19 and Table 7-20. The shunt electronics reliability (1-[the state 6 probability]) is written at the lower right of the printout. This figure for different configurations and failure rate combinations is graphically presented in Figure 7-42. As would be expected, the H and II configurations have different reliabilities depending upon which type (short or open) of element failure is most likely. However, for the range of λo to λs conceivable for this circuit, the reliability differences are too small to declare one configuration the best. The choice of configurations will be influenced most by operational considerations.

Remarks

The most unreliable part of the quad shunt is the resistor bank. In this application, the failure rates probably are not very representative of the failure assumed in this analysis. Relatively large changes in resistance (±20%) would not result in a failure in this application, but such drift out of tolerance did contribute to the failure rates. Hence, the values of the reliability for the quaded shunt are conservative.

Table 7-19. Quad Shunt Reliability (H)

```
08/28/69  8.348
 MISSION TIME IN YEARS=10

  TYPE IN LAMBDAS IN FAILURES PER MILLION HOURS
     RESISTOR, SHUNT(OPEN), SHUNT(SHORT)= 0.09, 0.226, 0.346   (Expected)

 NUMBER RESISTORS IN PARALLEL, NUMBER ALLOWED TO FAIL= 6, 2

  QUAD CENTER CONNECTED?=YES, (H CONFIGURATION)


 RESISTOR BANK RELIABILITY=    0.984336


    TRANSITION MATRIX FOR  87.660 HOURS
         1           2           3           4           5           6
  1 0.99979945 0.00006066 0.00003962 0.00006066 0.00003962 0.
  2 0.         0.99989972 0.         0.         0.00003962 0.00006066
  3 0.         0.00003033 0.99984958 0.00006066 0.00003962 0.00001980
  4 0.         0.         0.00003962 0.99989972 0.         0.00006066
  5 0.         0.00006066 0.00003962 0.00003033 0.99984958 0.00001980
  6 0.         0.         0.         0.         0.         1.00000000


       STATE MATRIX
  YRS      1           2           3           4           5           6

 0.      1.000000    0.          0.          0.          0.          0.

 1.00    0.980142    0.005994    0.003913    0.005994    0.003913    0.000044

 2.00    0.960678    0.011845    0.007730    0.011845    0.007730    0.000175

 3.00    0.941601    0.017555    0.011451    0.017555    0.011451    0.000391

 4.00    0.922903    0.023127    0.015078    0.023127    0.015078    0.000690

 5.00    0.904576    0.028565    0.018615    0.028565    0.018615    0.001070

 6.00    0.886613    0.033870    0.022062    0.033870    0.022062    0.001529

 7.00    0.869006    0.039046    0.025422    0.039046    0.025422    0.002065

 8.00    0.851749    0.044094    0.028696    0.044095    0.028696    0.002676

 9.00    0.834835    0.049019    0.031887    0.049019    0.031887    0.003361

10.00    0.818257    0.053822    0.034995    0.053822    0.034995    0.004117
                                                                    0.995883

     *****TOTAL OVERALL RELIABILITY= 0.9802913*****
```

Table 7-20. Quad Shunt Reliability (II)

```
08/28/69  8.420
 MISSION TIME IN YEARS=10

  TYPE IN LAMBDAS IN FAILURES PER MILLION HOURS
     RESISTOR, SHUNT(OPEN), SHUNT(SHORT)= 0.09, 0.226, 0.343\6

 NUMBER RESISTORS IN PARALLEL, NUMBER ALLOWED TO FAIL= 6, 2

  QUAD CENTER CONNECTED?= NO, (III CONFIGURATION)


 RESISTOR BANK RELIABILITY=    0.984336


    TRANSITION MATRIX FOR  87.660 HOURS
        1           2           3           4           5           6
 1 0.99979945 0.00006066 0.00003962 0.00006066 0.00003962 0.
 2 0.         0.99984958 0.00001981 0.00006066 0.00003962 0.00003032
 3 0.         0.         0.99989972 0.00006066 0.         0.00003962
 4 0.         0.00006066 0.00003962 0.99984958 0.00001981 0.00003032
 5 0.         0.00006066 0.         0.         0.99989972 0.00003962
 6 0.         0.         0.         0.         0.         1.00000000


       STATE MATRIX
 YRS      1           2           3           4           5           6

 0.       1.000000    0.          0.          0.          0.          0.

 1.00     0.980142    0.005991    0.003921    0.005991    0.003921    0.000033

 2.00     0.960678    0.011834    0.007761    0.011834    0.007761    0.000134

 3.00     0.941601    0.017531    0.011521    0.017531    0.011521    0.000299

 4.00     0.922903    0.023085    0.015201    0.023085    0.015202    0.000528

 5.00     0.904576    0.028500    0.018805    0.028500    0.018805    0.000819

 6.00     0.886613    0.033779    0.022333    0.033779    0.022333    0.001170

 7.00     0.869006    0.038924    0.025786    0.038924    0.025786    0.001581

 8.00     0.851749    0.043938    0.029166    0.043938    0.029166    0.002050

 9.00     0.834835    0.048825    0.032474    0.048825    0.032474    0.002575

10.00     0.818257    0.053586    0.035712    0.053586    0.035712    0.003156
                                                                    0.996844

     *****TOTAL OVERALL RELIABILITY= 0.9812377*****
```

Conclusions

Probability of success numbers for the two configurations were calculated as previously described. All calculations were done assuming a ten year mission. The exact mission time is not significant for this analysis since the numbers being calculated were for comparison only.

Figure 7-43 graphically presents this comparison. The multiple shunt circuits basic (no failure) reliability is .9388. Allowing one failure results in a reliability of .9864, but this is a definite reduction in available power since only failures short were included. The amount of power would be approximately one-eighth the difference between maximum initial power and the minimum initial load, which, assuming the shunt does not have to control the bus with no spacecraft loads applied, is 258/8=32 watts for an end of life capability of around 300 watts. This represents a 10% decrease in power which would seriously impact the number of science loads which could be powered. The quaded shunt, however, has a reliability of .980 which is no loss of power. Since the spacecraft is end of life power limited, a loss of power to achieve reliability is not an accepted trade, especially when the quad shunt provides a significantly higher reliability for no power loss over the multiple shunt scheme (.980 versus .939). In addition, allowing one failure in the multiple shunt scheme does not result in a significant gain over the quad shunt (.986 versus .980). Thus the quad shunt is the preferred approach from a reliability consideration.

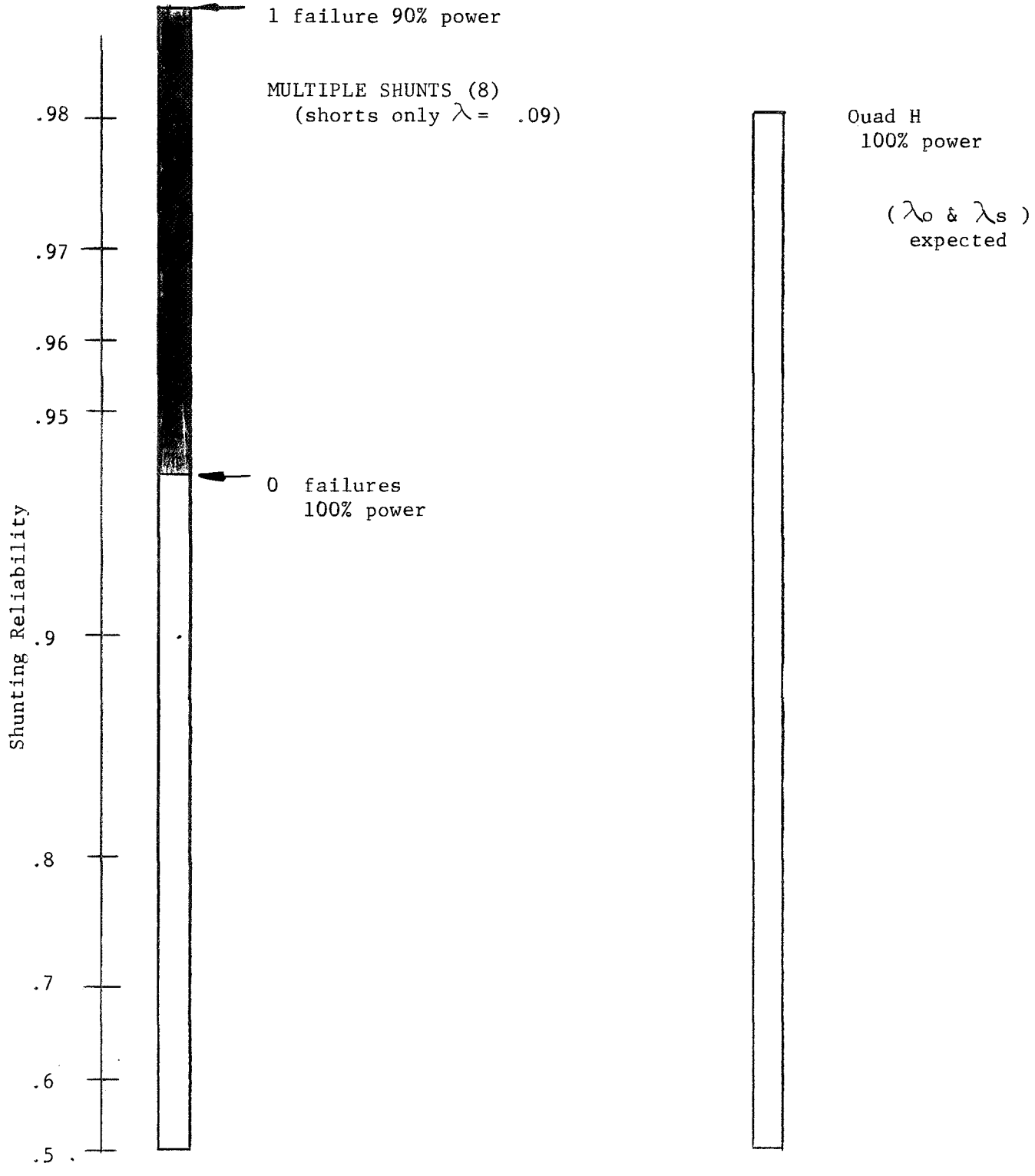


Figure 7-43. Comparative Shunt Regulator Reliability

SECTION 8. CONCLUSIONS

The stage of this effort does not permit any firm conclusions to be drawn at this time.

SECTION 9. RECOMMENDATIONS

Based on analyses completed to date, several areas for a change in requirements appear to be necessary or desirable.

1. It is recommended that all electrical power be distributed as direct current, and inverted at the using subsystem or converted within the using equipment to increase the overall reliability of the electrical power subsystem.

2. It is recommended that the requirement for conditioning of pressure signals from the RTG's be deleted, since this is neither desired nor required by the RTG.

SECTION 10. NEW TECHNOLOGY

No items of new technology have been identified during the period covered by this report.

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